SNx5DP149 3.4 Gbps DP++ to HDMI Retimer

1 Features

- DisplayPort™ Physical Layer Input Port to TMDS Physical Layer Output Port Supporting up to 3.4-Gbps Data Rates
- Support DisplayPort Dual-Mode Standard Version 1.1
- Support HDMI1.4b Transmitter Electrical Parameters
- Integrated TMDS Level Translator and CDR
- Adaptive Receiver Equalizer and Programmable Fixed Equalizer
- Selectable De-Emphasis
- Low Power Typical Consumption
  - 390 mW at 3.4-Gbps Retimer
  - 10 mW at Shutdown State
- Integrated DVI and HDMI Identification Recognition Dual Mode DP Type 2 Capability
- Active I^2C[4] Buffer
- Input Swap on Main Lanes
- I^2C[4] and Pin-Strap Programmable
- Industrial Temperature Range: –40 to 85°C (SN65DP149)
- Extended Commercial Temperature Range: 0 to 85°C (SN75DP149)
- 40-Pin 0.4-mm Pitch, 5-mm × 5-mm WQFN

2 Applications

- Personal Computer Market
- Next Generation Adaptor Dongles
- Desktop PC
- Notebook PC Market
- Docking Station
- HDTV
- Standalone Video Card
- Tablet

3 Description

The SNx5DP149 device is a dual mode[1] DisplayPort to transition-minimized differential signal (TMDS) retimer supporting digital video interface (DVI) 1.0 and high-definition multimedia interface (HDMI) 1.4b output signals. The SNx5DP149 device supports the dual mode standard version 1.1 type 1 and type 2 through the DDC link. The SNx5DP149 device supports data rate up to 3.4-Gbps per data lane to support Ultra HD (4K × 2K / 30-Hz) 8-bits per color high-resolution video and HDTV with 16-bit color depth at 1080p (1920 × 1080 / 60-Hz). The SNx5DP149 device can automatically configure itself as a re-driver at data rates <1 Gbps, or as a retimer at more than this data rate. This feature can be turned off through I^2C[4] programming.

For signal integrity, the SNx5DP149 device implements several features. The SNx5DP149 receiver supports both adaptive and fixed equalization to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. When working as a retimer, the embedded clock data recovery (CDR) cleans up the input high frequency and random jitter from video source. The transmitter provides several features for passing compliance and reducing system-level design issues like de-emphasis, which compensates for the attenuation when driving long cables or high-loss board traces. The SNx5DP149 device also includes TMDS output amplitude adjust using an external resistor on the Vsadj pin, source termination selection, and output slew rate control. Device operation and configuration can be programmed by pin strapping or I^2C[4].

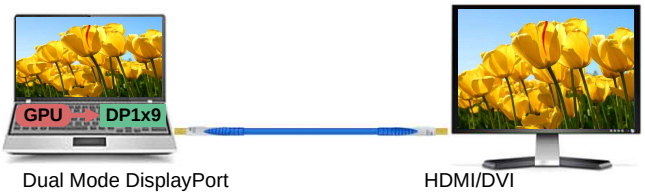
The SNx5DP149 device implements several methods for power management and active power reduction.

Device Information(1)

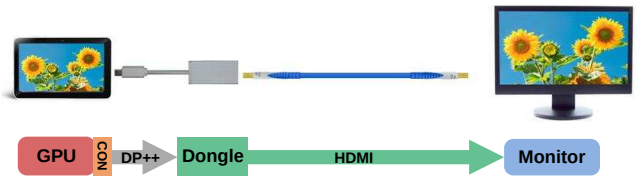
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65DP149 SN75DP149	WQFN (40)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

DP149 Mother Board Application Structure



DP149 Dongle Application Structure



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4 Revision History

Date	Revision	Notes
September 2015	*	Initial Release

5 Description (continued)

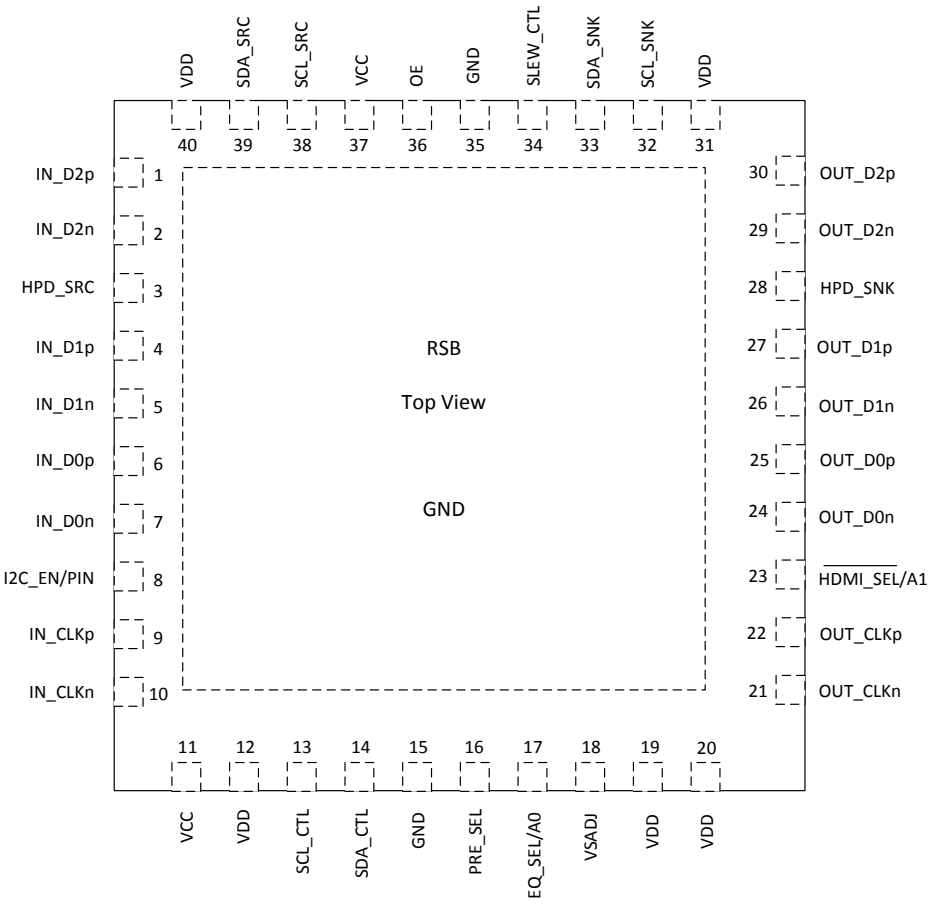
The SNx5DP149 receiver comes in a 40-pin RSB supporting space-constrained applications.

The SN65DP149 device is characterized for an industrial operational temperature range from –40°C to 85°C.

The SN75DP149 device is characterized for an extended commercial operational temperature range from 0°C to 85°C.

6 Pin Configuration and Functions

RSB Package
40-Pin WQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION (1)
SIGNAL NAME	NO.		
MAIN LINK INPUT PINS (FAIL SAFE)			
IN_D2p IN_D2n	1 2	I	Channel 2 differential input
IN_D1p IN_D1n	4 5	I	Channel 1 differential input
IN_D0p IN_D0n	6 7	I	Channel 0 differential input
IN_CLKp IN_CLKn	9 10	I	Clock differential input

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Pin Functions (continued)

PIN		I/O	DESCRIPTION (1)
SIGNAL NAME	NO.		
MAIN LINK OUTPUT PINS (FAIL SAFE)			
OUT_D2n OUT_D2p	29 30	O	TMDS data 2 differential output
OUT_D1n OUT_D1p	26 27	O	TMDS data 1 differential output
OUT_D0n OUT_D0p	24 25	O	TMDS data 0 differential output
OUT_CLKn OUT_CLKp	21 22	O	TMDS data clock differential output
HOT PLUG DETECT PINS			
HPD_SRC	3	O	Hot plug detect output
HPD_SNK	28	I (Failsafe)	Hot plug detect input
DDC DATA PINS			
SDA_SRC SCL_SRC	39 38	I/O (Failsafe)	Source side TMDS port bidirectional DDC data line
SDA_SNK SCL_SNK	33 32	I/O (Failsafe)	Sink side TMDS port bidirectional DDC data lines
CONTROL PINS			
OE	36	I	Operation enable/reset pin OE = L: Power-down mode OE = H: Normal operation Internal weak pullup: Resets device when transitions from H to L
SLEW_CTL	34	I 3 level (1)	Slew rate control when I2C_EN/PIN = Low. SLEW_CTL = H, fastest data rate (default) SLEW_CTL = L, 5-ps slow SLEW_CTL = No Connect, 10-ps slow When I2C_EN/PIN = High Slew rate is controlled through I^2C[4]
PRE_SEL	16	I 3 level (1)	PRE_SEL = L: - 2-dB de-emphasis PRE_SEL = No Connect: 0-dB PRE_SEL = H: Reserved Note: (3 level for pin strap programming, but 2 level when I^2C[4] address)
EQ_SEL/A0	17	I 3 level (1)	Input Receive Equalization pin strap when I2C_EN/PIN = Low EQ_SEL = L: Fixed EQ at 7.5-dB EQ_SEL = No Connect: Adaptive EQ EQ_SEL = H: Fixed at 14-dB When I2C_EN/PIN = High Address bit 1 Note: (3 level for pin strap programming but 2 level when I^2C[4] address)
I2C_EN/PIN	8	I	I2C_EN/PIN = High; puts device into I^2C control mode I2C_EN/PIN = Low; puts device into pin strap mode
SCL_CTL	13	I	I^2C clock signal Note: When I2C_EN/PIN = Low Pin strapping take priority and those functions cannot be changed by I^2C
SDA_CTL	14	I/0	I^2C data signal Note: When I2C_EN/PIN = Low Pin strapping take priority and those functions cannot be changed by I^2C
Vsadj	18	I	TMDS-compliant voltage swing control nominal resistor to GND
$\overline{\text{HDMI\_SEL}}$/A1	23	I	$\overline{\text{HDMI\_SEL}}$ when I2C_EN/PIN = Low $\overline{\text{HDMI\_SEL}}$ = High: Device configured for DVI $\overline{\text{HDMI\_SEL}}$ = Low: Device configured for HDMI (Adaptor ID block is readable through I^2C When I2C_EN/PIN = High Address bit 2 Note: Weak internal pull down
SUPPLY AND GROUND PINS			
V_{CC}	11, 37	P	3.3-V power supply
V_{DD}	12, 19, 20, 31, 40	P	1.1-V power supply

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Pin Functions (continued)

PIN		I/O	DESCRIPTION (1)
SIGNAL NAME	NO.		
GND	15, 35, Thermal Pad	—	Ground

(1) (H) Logic high (pin strapped to VCC through 65-kΩ resistor); (L) logic low (pin strapped to GND through 65-kΩ resistor); (for mid-level, no connect)

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
Supply voltage(3)	V_{CC}	–0.3	4	V
	V_{DD}	–0.3	1.4	V
Voltage	Main link input (IN_Dx AC-coupled mode)		1.56	V
	TMDS outputs (OUT_Dx)	–0.3	4	V
	HPD_SRC, Vsadj, SDA_CTL, SCL_CTL, OE, $\overline{\text{HDMI\_SEL}}$/A1, EQ_SEL/A0, I2C_EN/PIN, SLEW_CTL, SDA_SRC, SCL_SRC	–0.3	4	V
	HPD_SNK, SDA_SNK, SCL_SNK	–0.3	6	V
Continuous power dissipation		See *Thermal Information*		
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-B.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
GENERAL PARAMETERS						
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{DD}			1.00	1.1	1.27	
T_{CASE}	Case temperature for RSB package				93.5	°C
T_A	Operating free-air temperature	SN75DP149	0		85	°C
		SN65DP149	–40		85	
MAIN LINK DIFFERENTIAL PINS						
V_{ID_PP}	Peak-to-peak input differential voltage		75		1200	mV
V_{IC}	Input common mode voltage		0		2	V
C_{AC}	AC coupling capacitance		75	100	200	nF
d_R	Data rate		0.25		3.4	Gbps
Vsadj	TMDS-compliant swing voltage bias resistor			7.06		kΩ
DDC AND I^2C PINS AND CONTROL PINS						
$V_{I\text{-}DC}$	DC input voltage	HPD_SNK, SCL/SDA_SNK	–0.3		5.5	V
		All other DDC, local I^2C, and control pins	–0.3		3.6	V
V_{IL}	Low-level input voltage at DDC/I^2C and HPD				0.8	V
	Low-level input voltage at SLEW_CTL, PRE_SEL, EQ_SEL/A0, SWAP/POL				0.3	
V_{IM}	No connect input voltage at SLEW_CTL, PRE_SEL, EQ_SEL/A0, SWAP/POL		1	1.2	1.4	V
V_{IH}	High-level input voltage at HPD		2			V
	High-level input voltage at SCL_SRC, SDA_SRC, I^2C		1.8			
	High-level input voltage at SCL_SNK, SDA_SNK		2.8			
	High-level input voltage at SLEW_CTL, PRE_SEL, EQ_SEL/A0, SWAP/POL		2.6			
V_{OL}	Low-level output voltage				0.4	V
V_{OH}	High-level output voltage		2.4			V
f_{SCL}	SCL clock frequency fast I^2C mode for local I^2C control			400		kHz
C_{bus}	Total capacitive load for each bus line (DDC and local I^2C pins)				400	pF
$d_{R(DDC)}$	DDC data rate			100	400	kbps
I_{IH}	High-level input current		–30		30	µA
I_{IL}	Low-level input current		–10		10	µA
I_{OS}	Short circuit output current		–50		50	mA
I_{OZ}	High impedance output current				10	µA
R_{OEPU}	Pullup resistance on OE pin		150		250	kΩ

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7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		SNx5DP149 RSB (WQFN) 40 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance (High-K board(2))	9.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance (High-K board(2))	23.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-case (bottom) thermal resistance	3.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Test conditions for Ψ_{JB} and Ψ_{JT} are clarified in TI document SPRA953, *Semiconductor and IC Package Thermal Metrics*.

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7.5 Power Supply Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
P_{D1}	Device power dissipation (retimer mode)	OE = H, $\overline{HDMI\_SEL}$ = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ IN_Dx: V_{ID_PP} = 1200-mV, 3.4-Gbps TMDS pattern AUX: V_I = 3.3-V I2C_EN/PIN = L, PRE_SEL= H, IN_EQ_CTL= H, SDA_CTL/CLK_CTL = 0-V		390	510	mW
P_{D2}	Device power dissipation (redriver mode)	OE = H, $\overline{HDMI\_SEL}$ = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ IN_Dx: V_{ID_PP} = 1200-mV, 3.4-Gbps TMDS pattern AUX: V_I = 3.3-V I2C_EN/PIN = L, PRE_SEL= H, IN_EQ_CTL= H, SDA_CTL/CLK_CTL = 0-V		225	350	mW
P_{SD1}	Device power with shut down OE = L	OE = L, V_{CC} = 3.3/3.6 V, V_{DD} = 1.1/1.27 V, VSadj = 7.06 kΩ		5	15	mW
I_{DD1}	V_{DD} Supply current (TMDS 3.4-Gpbs retimer mode)	OE = H, $\overline{HDMI\_SEL}$ = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ IN_Dx: VID_PP = 1200-mV, 3.4-Gbps TMDS pattern AUX: VI = 3.3-V, 100-kHz PRBS I2C_EN/PIN = L, PRE_SEL = H, IN_EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V, SLEW_CTL = H		250	300	mA
I_{CC1}	V_{CC} Supply current (TMDS 3.4-Gpbs retimer mode)	OE = H, $\overline{HDMI\_SEL}$ = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ IN_Dx: VID_PP = 1200-mV, 3.4-Gbps TMDS pattern AUX: VI = 3.3-V, 100-kHz PRBS I2C_EN/PIN = L, PRE_SEL = H, IN_EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V, SLEW_CTL = H		35	50	mA
I_{DD2}	V_{DD} Supply current (TMDS 3.4-Gpbs redriver mode)	OE = H, $\overline{HDMI\_SEL}$ = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ IN_Dx: V_{ID_PP} = 1200-mV, 3.4-Gbps TMDS pattern AUX: VI = 3.3-V, 100-kHz PRBS I2C_EN/PIN = L, PRE_SEL = H, IN_EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V, SLEW_CTL = H		170	200	mA
I_{CC2}	V_{CC} Supply current (TMDS 3.4-Gpbs redriver mode)	OE = H, $\overline{HDMI\_SEL}$ = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ IN_Dx: VID_PP = 1200-mV, 3.4-Gbps TMDS pattern AUX: VI = 3.3-V, 100-kHz PRBS I2C_EN/PIN = L, PRE_SEL = H, IN_EQ_CTL = H, SDA_CTL/CLK_CTL = 0 V, SLEW_CTL = H		8	20	mA
I_{SD1}	V_{DD} Shutdown current	OE = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ		3	10.5	mA
I_{SD1}	V_{CC} Shutdown current	OE = L, V_{CC} = 3.3/3.6-V, V_{DD} = 1.1/1.27-V, VSadj = 7.06-kΩ		2	5	mA

(1) The typical rating is simulated at 3.3-V V_{CC} and 1.1-V V_{DD} and at 27°C temperature unless otherwise noted

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7.6 Differential Input Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$D_{R\_RX\_DATA}$	Ddata lanes data rate		0.25		3.4	Gbps
$D_{R\_RX\_CLK}$	Clock lanes clock rate		25		340	MHz
t_{RX_DUTY}	Input clock duty circle		40%	50%	60%	
t_{CLK_JIT}	Input clock jitter tolerance				0.3	Tbit
t_{DATA_JIT}	Input data jitter tolerance	Test the TTP2, see Figure 7			150	ps
T_{RX_INTRA}	Input intra-pair skew tolerance	Test at TTP2 when DR = 1.6-Gbps, see Figure 7	112			ps
T_{RX_INTER}	Input inter-pair skew tolerance				1.8	ns
$E_{QH(D)}$	Fixed EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0 = H; Fixed EQ gain, test at 3.4-Gbps		14		dB
$E_{QL(D)}$	Fixed EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0 = L; Fixed EQ gain, test at 3.4-Gbps		7.5		dB
$E_{QZ(D)}$	Adaptive EQ gain for data lane IN_D(0,1,2)n/p	EQ_SEL/A0 = Z; adaptive EQ	2		14	dB
$E_{Q(c)}$	EQ gain for clock lane IN_CLKn/p	EQ_SEL/A0 = H,L,NC		3		
R_{INT}	Input differential termination impedance		80	100	120	Ω
V_{ITERM}	Input termination voltage	OE = H		0.7		V
V_{ID_PP}	Input differential voltage (peak to peak)	Tested at TTP2, check Figure 7	75		1200	mV_{PP}

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7.7 HDMI and DVI TMDS Output Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Single-ended high level output voltage	Data rate ≤ 1.65-Gbps; PRE_SEL = NC; SLEW_CTL = H; OE = H; DR = 750-Mbps, VSadj = 7.06-kΩ	V_{CC} – 10		V_{CC} + 10	mV
		1.65-Gbps < Data rate ≤ 3.4-Gbps; PRE_SEL = NC; ; SLEW_CTL = H; OE = H; DR = 2.97-Gbps, VSadj = 7.06 kΩ	V_{CC} – 200		V_{CC} + 10	
V_{OL}	Single-ended low level output voltage	Data rate ≤ 1.65-Gbps; PRE_SEL = NC; SLEW_CTL = H; OE = H; DR = 750-Mbps, VSadj = 7.06-kΩ	V_{CC} – 600		V_{CC} – 400	mV
		1.65-Gbps < Data rate ≤ 3.4-Gbps; PRE_SEL = NC; SLEW_CTL = H; OE = H; DR = 2.97-Gbps, VSadj = 7.06-kΩ	V_{CC} – 700		V_{CC} – 400	
V_{SWING_DA}	Single-ended output voltage swing on data lane	PRE_SEL = NC; SLEW_CTL = H; OE = H; DR = 270-Mbs/2.97 VSadj = 7.06-kΩ	400	500	600	mV
V_{SWING_CLK}	Single-ended output voltage swing on clock lane	Data rate ≤ 3.4-Gbps; PRE_SEL = NC; SLEW_CTL = H; OE = H; VSadj = 7.06-kΩ	400	500	600	mV
ΔV_{SWING}	Change in single-end output voltage swing per 100 Ω ΔVsadj			20		mV
$\Delta V_{OCM(SS)}$	Change in steady state output common mode voltage between logic levels		–5		5	mV
$V_{OD(PP)}$	Output differential voltage before pre-emphasis	Vsadj = 7.06-kΩ; PRE_SEL = Z, See Figure 5	800		1200	mV
$V_{OD(SS)}$	Steady-state output differential voltage	Vsadj = 7.06-kΩ; PRE_SEL = L, See Figure 6	600		1050	mV
I_{LEAK}	Failsafe condition leakage current	V_{CC} = 0-V; V_{DD} = 0-V; output pulled to 3.3 V through 50-Ω resistors			45	µA
I_{OS}	Short circuit current limit	Main link output shorted to GND			50	mA
R_{TERM}	Source termination resistance for HDMI 2.0		75		150	Ω

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7.8 DDC, and I²C Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	SCL/SDA_CTL, SCL/SDA_SRC low-level input voltage				0.3 VCC	V
V_{IH}	SCL/SDA_CTL, SCL/SDA_SRC high-level input voltage		0.7 VCC		VCC + 0.5	V
V_{OL}	SCL/SDA_CTL, SCL/SDA_SRC low-level output voltage	I_0 = 3-mA and VCC > 2-V			0.4	V
		I_0 = 3-mA and VCC < 2-V			0.2 VCC	V

7.9 HPD Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	HPD_SNK	2.1			V
V_{IL}	Low-level input voltage	HPD_SNK			0.8	V
V_{OH}	High-level output voltage	I_{OH} = –500-µA; HPD_SRC	2.4		3.6	V
V_{OL}	Low-level output voltage	I_{OL} = 500-µA; HPD_SRC	0		0.1	V
I_{LEAK}	Failsafe condition leakage current	VCC = 0-V; V_{DD} = 0-V; HPD_SNK = 5-V			40	µA
I_{H_HPD}	High-level input current	Device powered; V_{IH} = 5-V; I_{H_HPD} includes R_{pdHPD} resistor current			40	µA
I_{L_HPD}	Low-level input current	Device powered; V_{IL} = 0.8-V; I_{L_HPD} includes R_{pdHPD} resistor current			30	
R_{pdHPD}	HPD input termination to GND	V_{CC} = 0-V	150	190	220	kΩ

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7.10 HDMI and DVI Main Link Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REDRIVER MODE						
D_R	Data rate (Automatic Mode)		250		1000	Mbps
D_R	Data rate (full redriver mode)		250		3400	Mbps
t_{PLH}	Propagation delay time (low to high)		250		600	ps
t_{PHL}	Propagation delay time (high to low)		250		800	ps
t_{T1}	Transition time (rise and fall time); measured at 20% and 80% levels for data lanes. TMDS clock meets t_{T3} for all three times.	SLEW_CTL = H; PRE_SEL = NC; OE = H; DR = 2.97 Gbps	75			ps
t_{T2}		SLEW_CTL = L; PRE_SEL = NC; OE = H; DR = 2.97 Gbps	75			
t_{T3}		SLEW_CTL = NC; PRE_SEL = NC; OE = H; DR = 2.97 Gbps; CLK 297MHz	100			
$t_{SK1(T)}$	Intra-pair output skew	SLEW_CTL = NC; PRE_SEL = NC; OE = H; DR = 2.97 Gbps;			40	ps
$t_{SK2(T)}$	Inter-pair output skew	SLEW_CTL = NC; PRE_SEL = NC; OE = H; DR = 2.97 Gbps;			100	
t_{JITD1}	Total output data jitter	DR = 2.97 Gbps, $\overline{\text{HDMI\_SEL}}$/A1 = NC, EQ_SEL/A0 = NC; PRE_SEL = NC; SLEW_CTL = H OE = H. See Figure 7 at TTP3			0.2	Tbit
t_{JITC1}	Total output clock jitter	CLK = 297 MHz			0.25	Tbit
RETIMER MODE						
d_R	Data rate (Full retimer mode)		0.25		3.4	Gbps
d_R	Data rate (Automatic mode)		1.0		3.4	Gbps
d_{XVR}	Automatic redriver to retimer crossover	Measured with input signal applied from 0 to 200 mVpp	.75	1.0	1.25	Gbps
$f_{CROSSOVER}$	Crossover frequency hysteresis			250		MHz
P_{LLBW}	Data retimer PLL bandwidth	Default loop bandwidth setting		.4	1	MHz
t_{ACQ}	Input clock frequency detection and retimer acquisition time			180		µs
I_{JT1}	Input clock jitter tolerance	Tested when data rate > 1.0 Gbps			0.3	Tbit
t_{T1}	Transition time (rise and fall time); measured at 20% and 80% levels for data lanes. TMDS clock meets t_{T3} for all three times.	SLEW_CTL = H; PRE_SEL = NC; OE = H; DR = 3.4 Gbps	75			ps
t_{T2}		SLEW_CTL = L; PRE_SEL = NC; OE = H; DR = 3.4 Gbps	75			
t_{T3}		SLEW_CTL = NC; PRE_SEL = NC; OE = H; DR = 3.4 Gbps; CLK = 297 MHz	100			
t_{DCD}	OUT_CLK ± duty cycle		40%	50%	60%	
t_{SK_INTER}	Inter-pair output skew	Default setting for internal inter-pair skew adjust, $\overline{\text{HDMI\_SEL}}$/A1 = NC			0.2	Tch
t_{SK_INTRA}					0.15	Tbit
$t_{JITC1(1.4b)}$	Total output clock jitter	CLK = 297 MHz			0.25	Tbit

7.11 HPD Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD(HPD)}$	Propagation delay from HPD_SNK to HPD_SRC; rising edge and falling edge	See Figure 10; not valid during switching time		40	120	ns
$t_{T(HPD)}$	HPD logical disconnected timeout	See Figure 11		2		ms

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7.12 DDC and I²C Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time of both SDA and SCL signals	Vcc = 3.3-V			300	ns
t_f	Fall time of both SDA and SCL signals				300	ns
t_{HIGH}	Pulse duration, SCL high		0.6			µs
t_{LOW}	Pulse duration, SCL low		1.3			µs
t_{SU1}	Setup time, SDA to SCL		100			ns
$t_{ST,\ STA}$	Setup time, SCL to start condition		0.6			µs
$t_{HD,STA}$	Hold time, start condition to SCL		0.6			µs
$t_{ST,STO}$	Setup time, SCL to stop condition		0.6			µs
$t_{(BUF)}$	Bus free time between stop and start condition.		1.3			µs
t_{PLH1}	Propagation delay time, low-to-high-level output	Source-to-sink: 100-kbps pattern; Cb(Sink) = 400-pF(1); See Figure 14		360		ns
t_{PHL1}	Propagation delay time, high-to-low-level output			230		ns
t_{PLH2}	Propagation delay time, low-to-high-level output	Sink to Source: 100-kbps pattern; Cb(Source) = 100-pF(1); See Figure 15		250		ns
t_{PHL2}	Propagation delay time, high-to-low-level output			200		ns

(1) Cb = total capacitance of one bus line in pF.

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7.13 Parameter Measurement Information

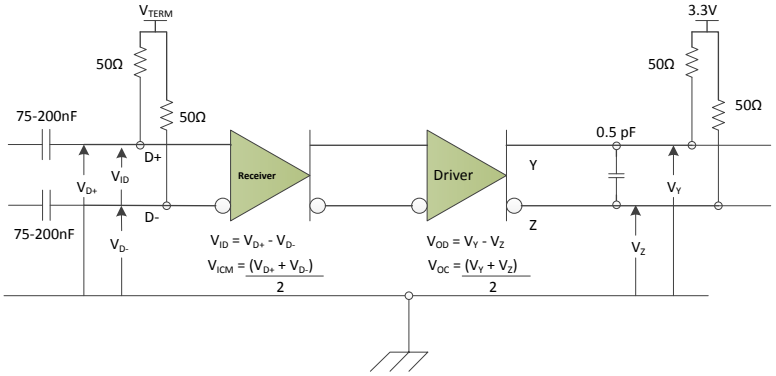


Figure 1. TMDS Main Link Test Circuit

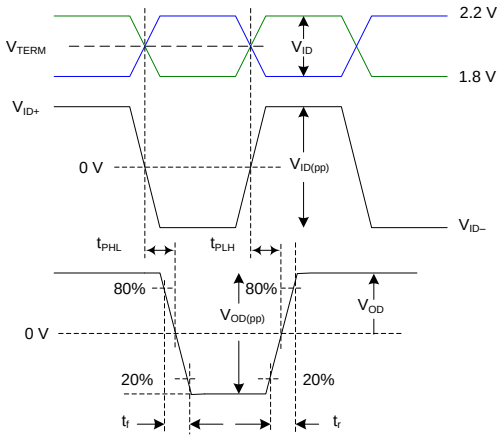


Figure 2. Input and Output Timing Measurements

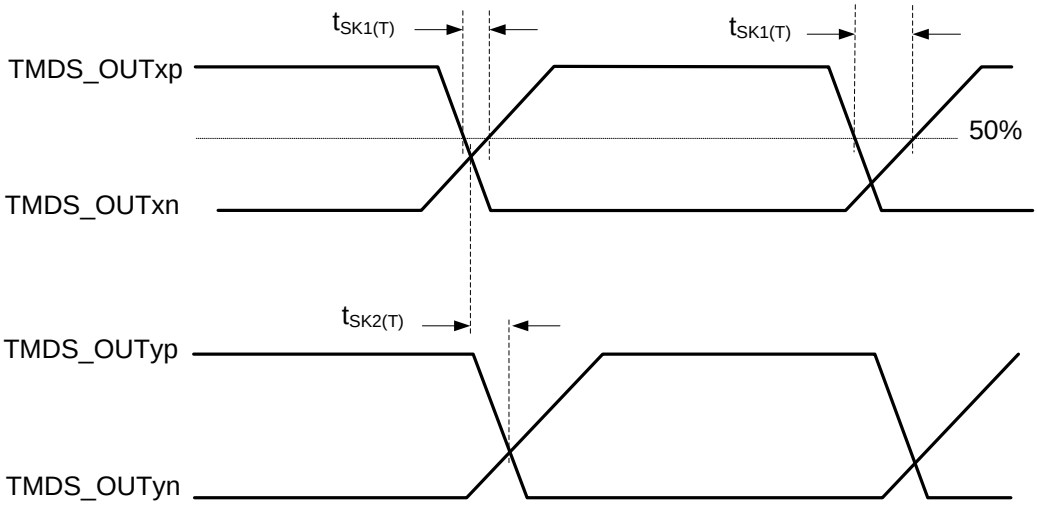


Figure 3. HDMI and DVI Sink TMDS Output Skew Measurements

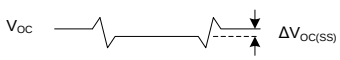


Figure 4. TMDS Main Link Common Mode Measurements

Parameter Measurement Information (continued)

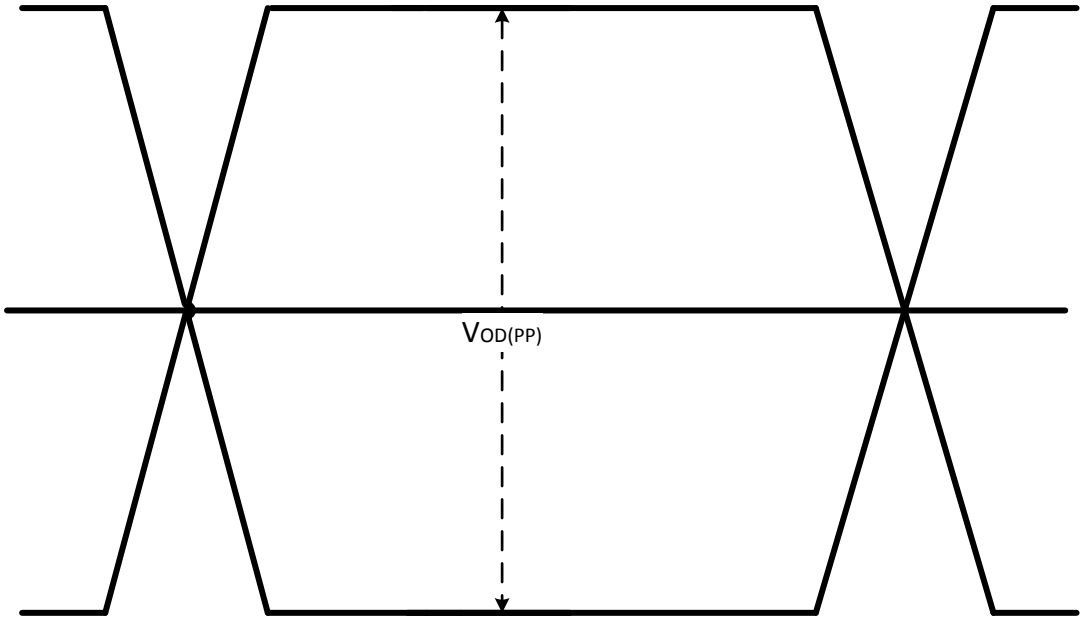


Figure 5. Output Differential Waveform 0 dB De-Emphasis

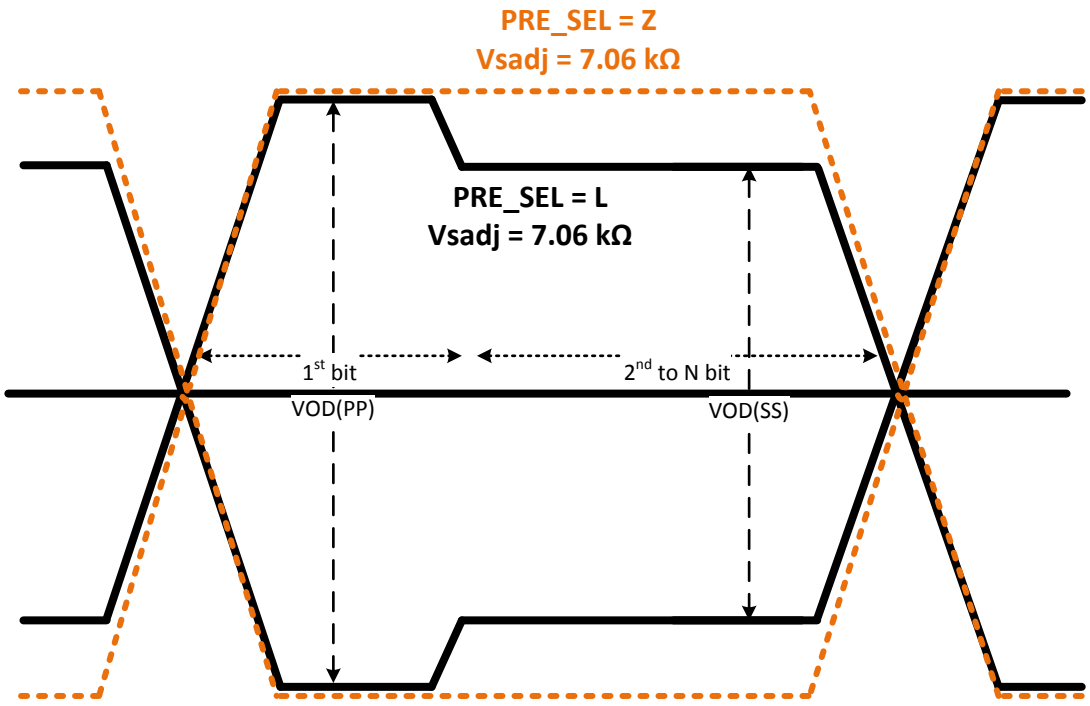
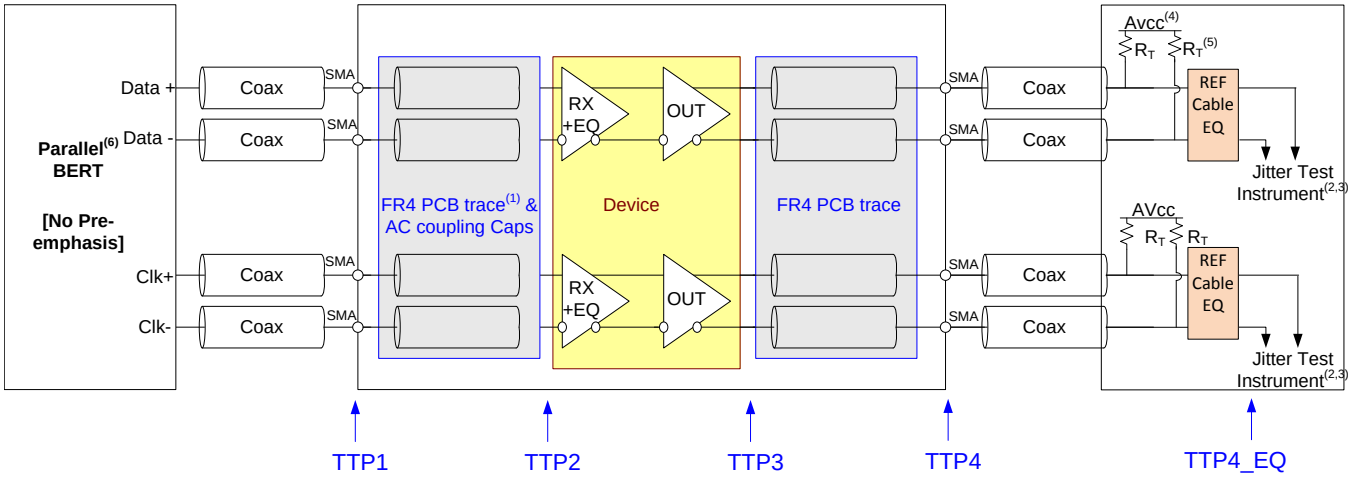


Figure 6. PRE_SEL = L for –2-dB De-Emphasis

Parameter Measurement Information (continued)



(1) The FR4 trace between TTP1 and TTP2 is designed to emulate 1-8" of FR4, AC coupling cap, connector and another 1-2" of FR4. Trace width – 4 mils. 100-Ω differential impedance.

(2) All jitter is measured at a BER of 10-9.

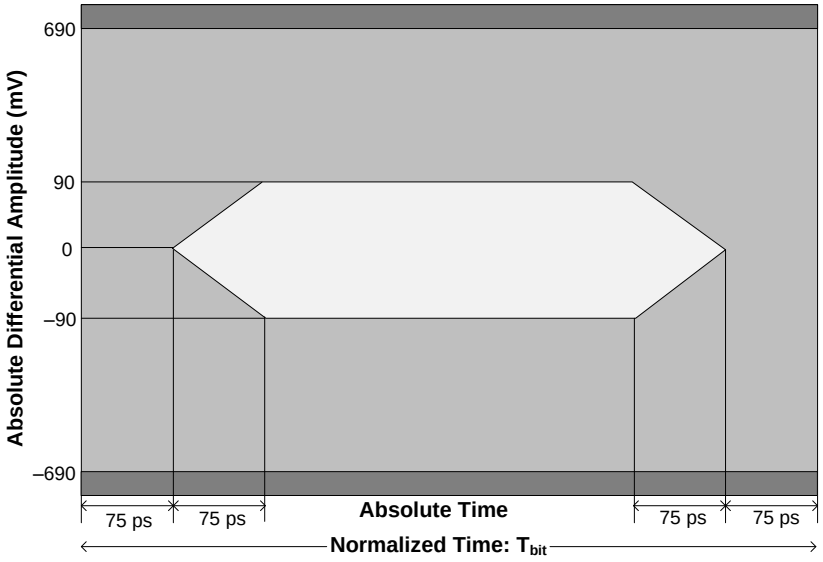
(3) Residual jitter reflects the total jitter measured at TTP4 minus the jitter measured at TTP1.

(4) AVCC = 3.3-V

(5) RT = 50-Ω

(6) The input signal from parallel bit error rate tester (BERT) does not have any pre-emphasis. Refer to *Recommended Operating Conditions*.

Figure 7. TMDS Output Jitter Measurement



TMDS data eye mask at connector for clock frequency over 165 MHz.

Figure 8. Input Eye Mask at TTP2

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Parameter Measurement Information (continued)

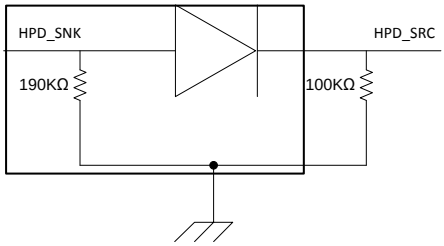

Figure 9. HPD Test Circuit

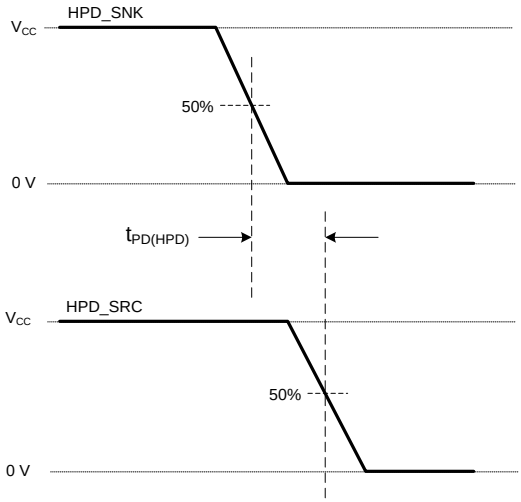

Figure 10. HPD Timing Diagram Number 1

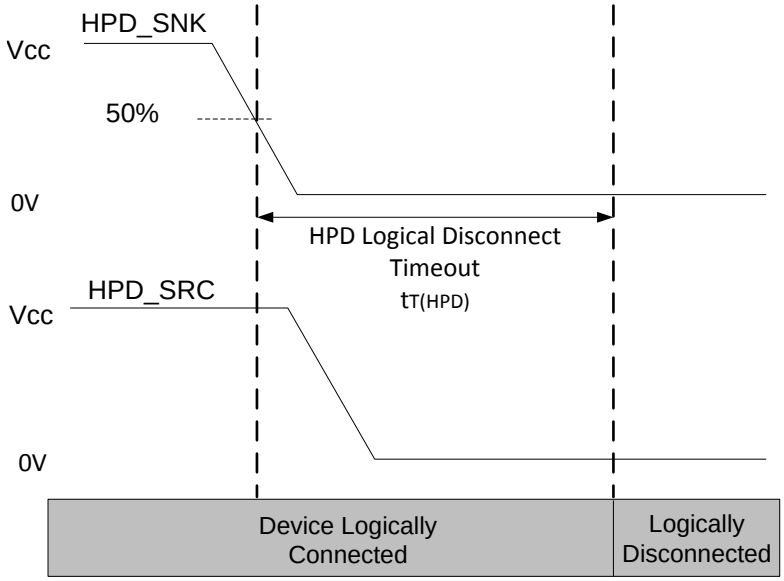

Figure 11. HPD Logic Disconnect Timeout

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Parameter Measurement Information (continued)

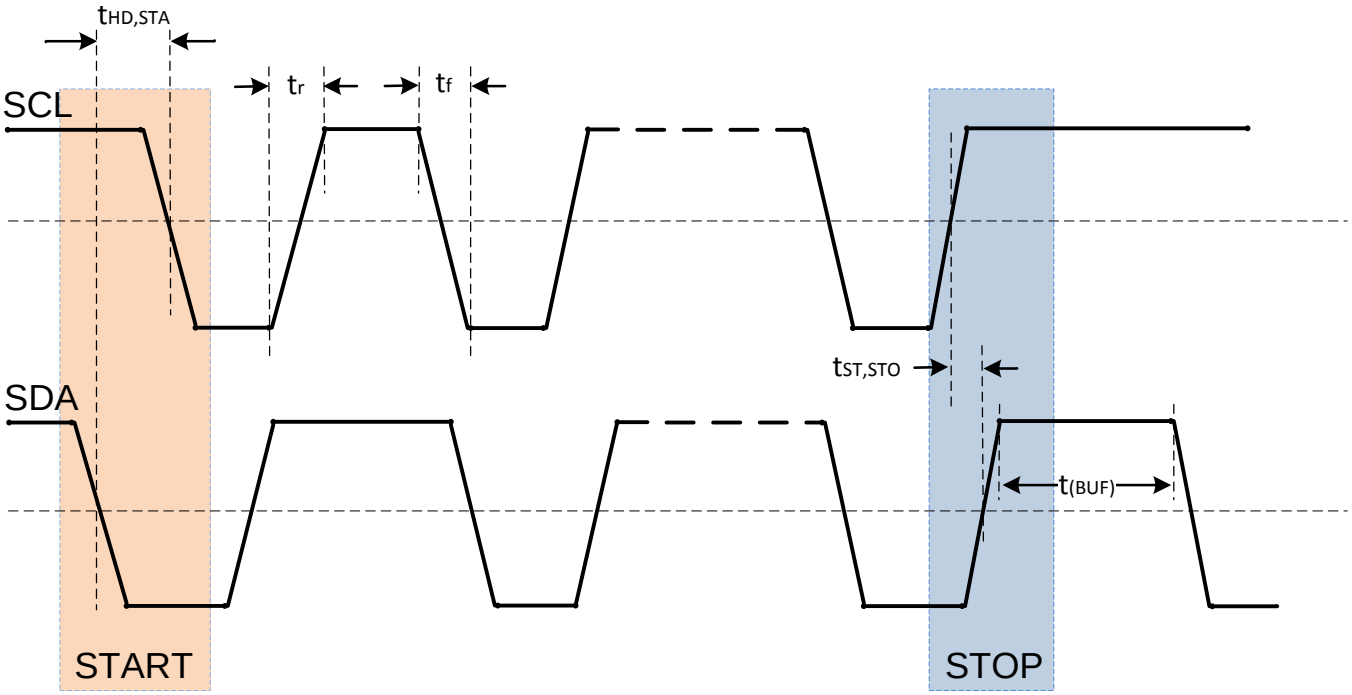

Figure 12. Start and Stop Condition Timing

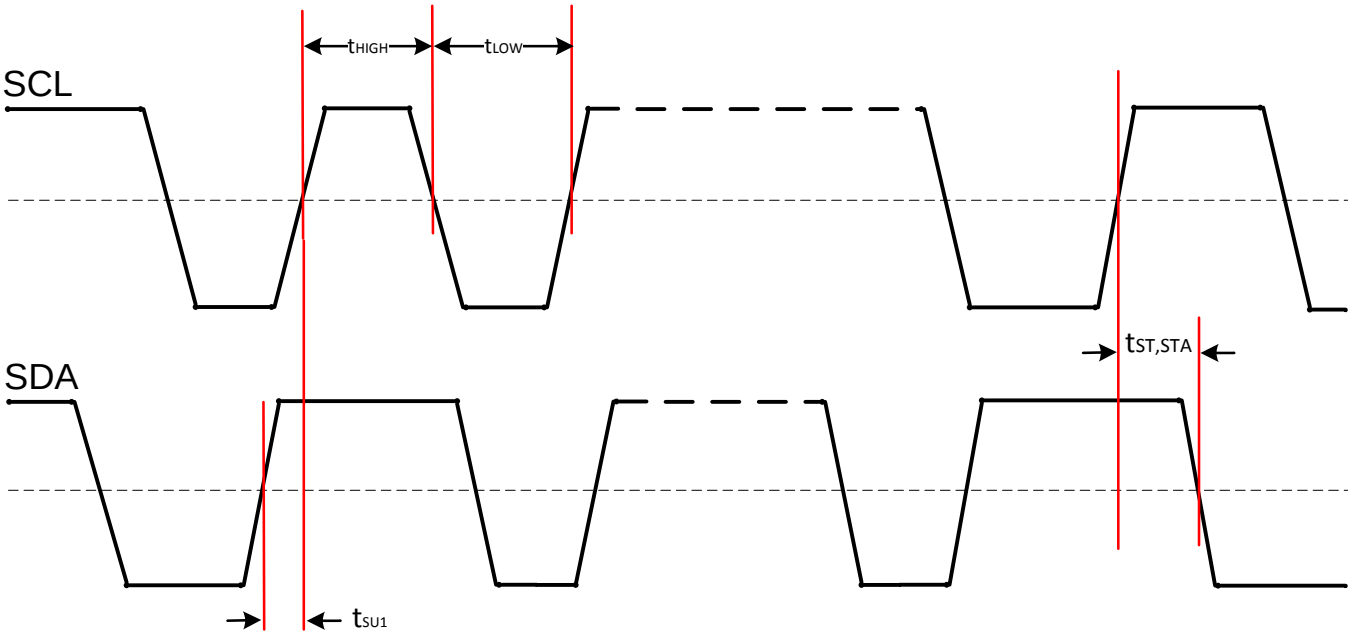

Figure 13. SCL and SDA Timing

Parameter Measurement Information (continued)

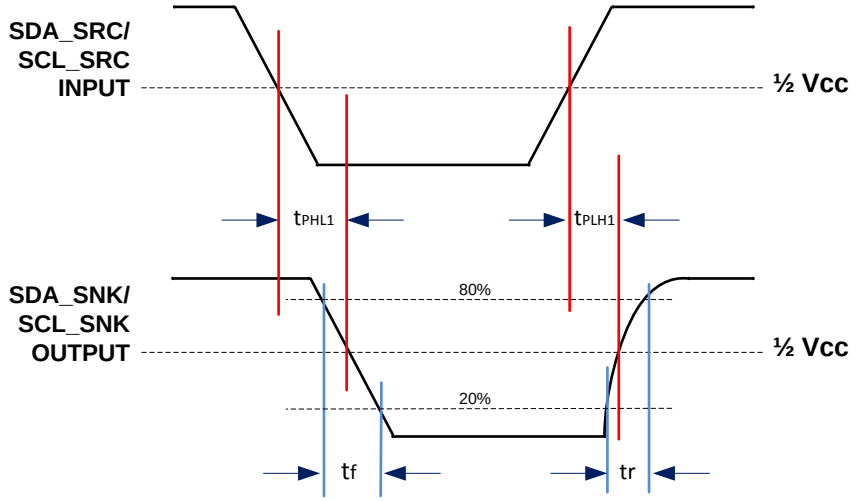

Figure 14. DDC Propagation Delay – Source to Sink

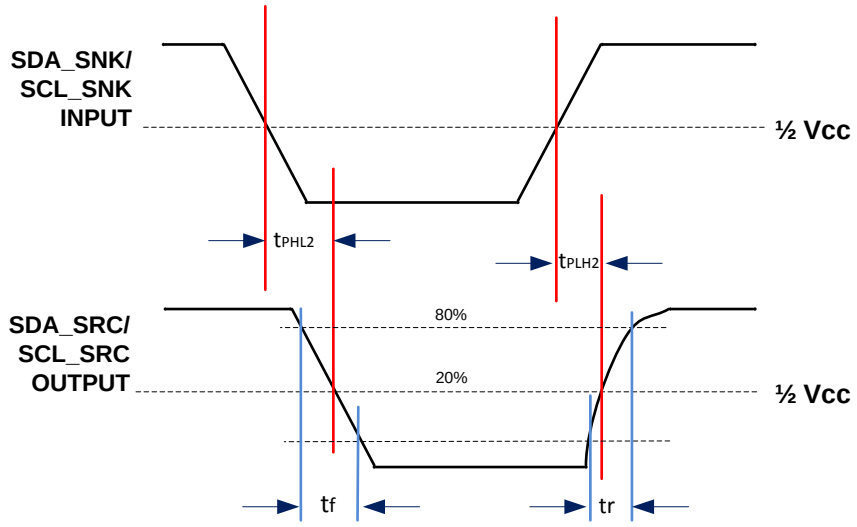

Figure 15. DDC Propagation Delay – Sink to Source

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7.14 Typical Characteristics

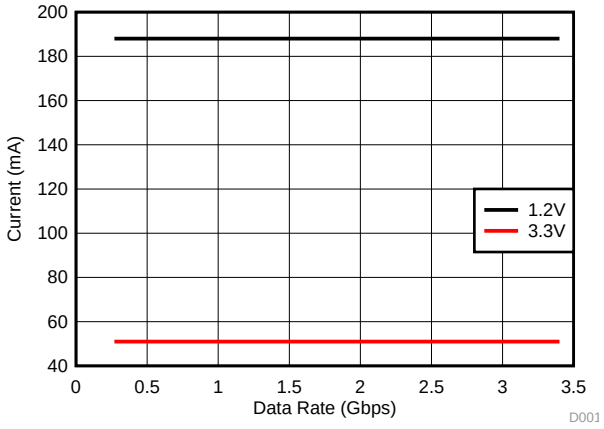

Figure 16. Current vs Data Rate in Retimer Mode

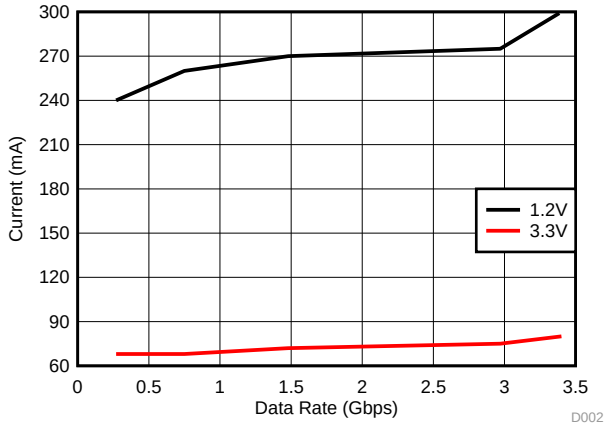

Figure 17. Current vs Data Rate in Redriver Mode

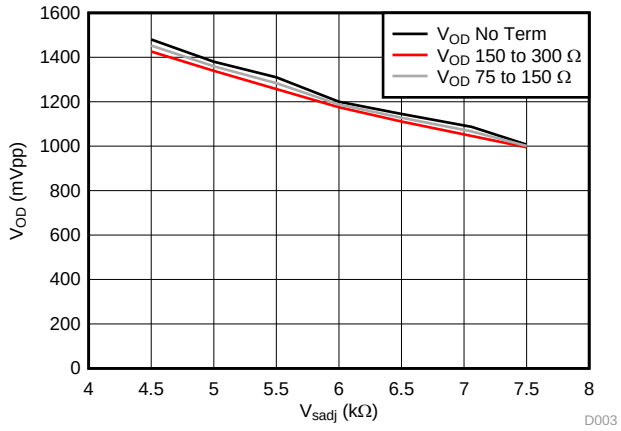

Figure 18. V_{OD} vs V_{sadj}

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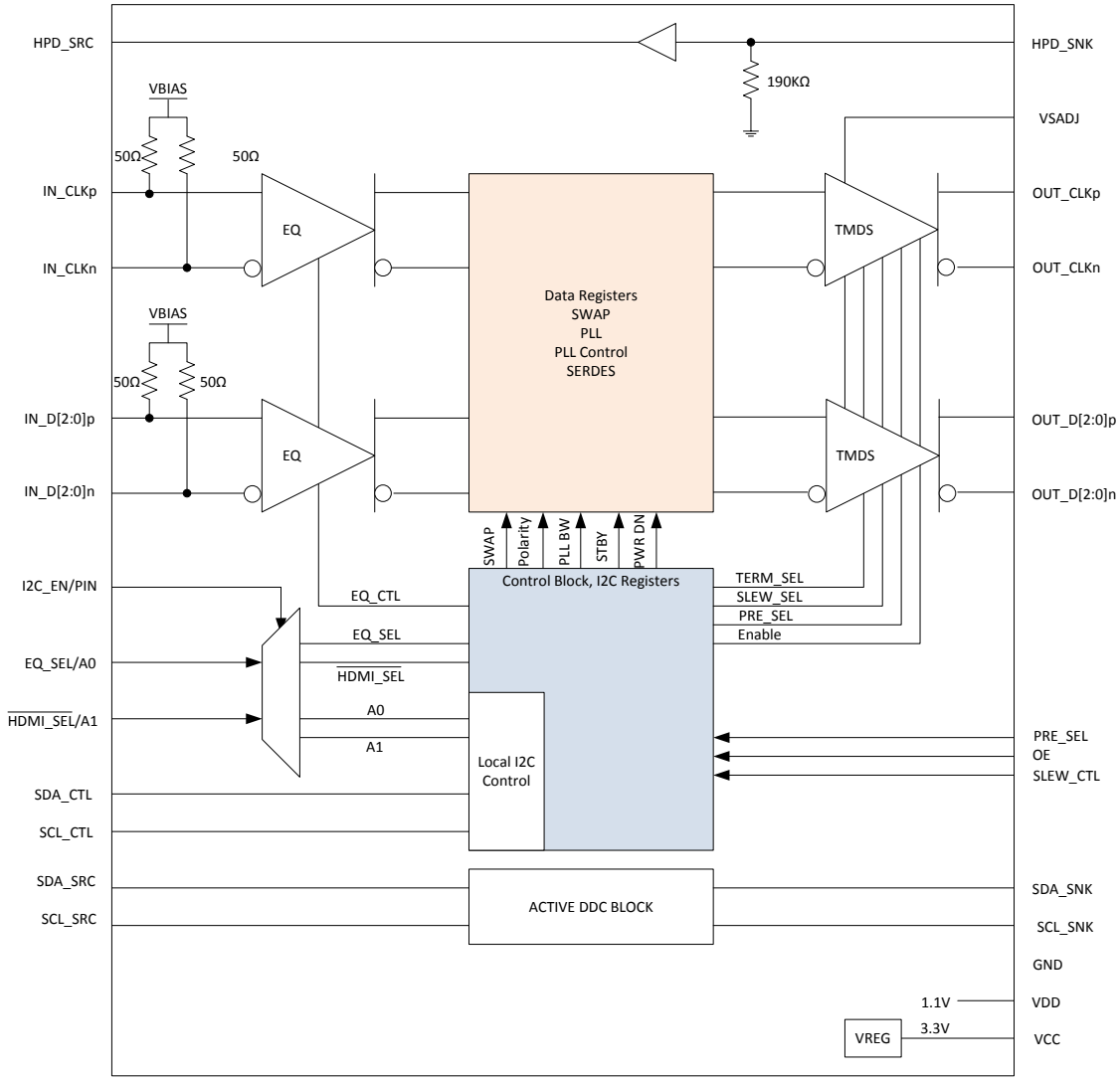
8 Detailed Description

8.1 Overview

The SNx5DP149 device is a Dual Mode[1] DisplayPort retiming level shifter that supports data rates up to 3.4-Gbps for HDMI1.4b. The device takes in AC coupled HDMI/DVI signals and level shifts them to TMDS signals while compensating for loss and jitter through its receiver equalizer and retiming functions. The SNx5DP149 in default configuration should meet most system needs but also provides features that allow the system implementer flexibility in design. Programming can be accomplished through I^2C[4] or pin strapping.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Reset Implementation

When OE is de-asserted, control signal inputs are ignored; the Dual Mode[1] DisplayPort inputs and outputs are high impedance. It is critical to transition the OE input from a low level to a high level after the V_{CC} supply has reached the minimum recommended operating voltage. Achieve this transition by a control signal to the OE input, or by an external capacitor connected between OE and GND. To ensure that the SNx5DP149 device is properly reset, the OE pin must be de-asserted for at least 100-µs before being asserted. When OE is toggled in this manner the device is reset. This requires the device to be reprogrammed if it was originally programmed

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Feature Description (continued)

through I^2C for configuration. When implementing the external capacitor, the size of the external capacitor depends on the power-up ramp of the V_{CC} supply, where a slower ramp-up results in a larger value external capacitor. Refer to the latest reference schematic for SNx5DP149; consider approximately 200-nF capacitor as a reasonable first estimate for the size of the external capacitor. Both OE implementations are shown in Figure 19 and Figure 20.

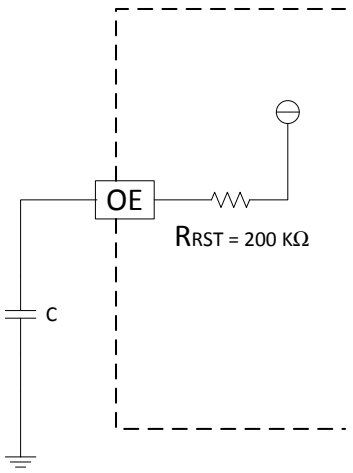

Figure 19. External Capacitor Controlled OE

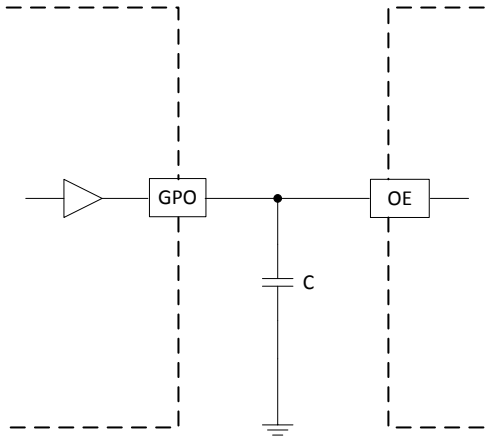

Figure 20. OE Input from Active Controller

8.3.2 Operation Timing

SNx5DP149 starts to operate after the OE signal goes high (see Figure 21, Figure 22, and Table 1). Keeping OE low until V_{DD} and V_{CC} become stable avoids any timing requirements as shown in Figure 21.

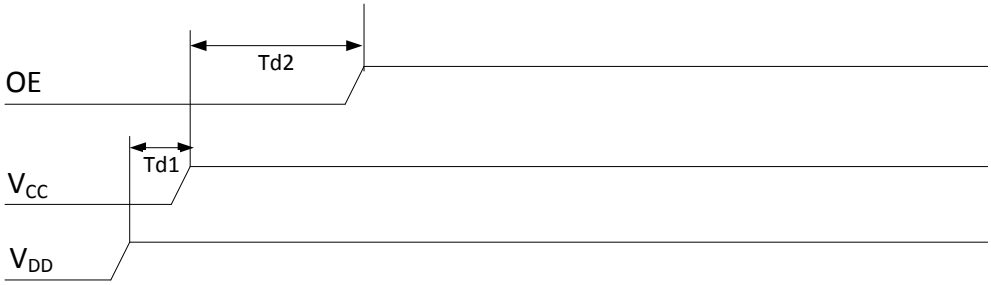

Figure 21. Power-Up Timing for SNx5DP149

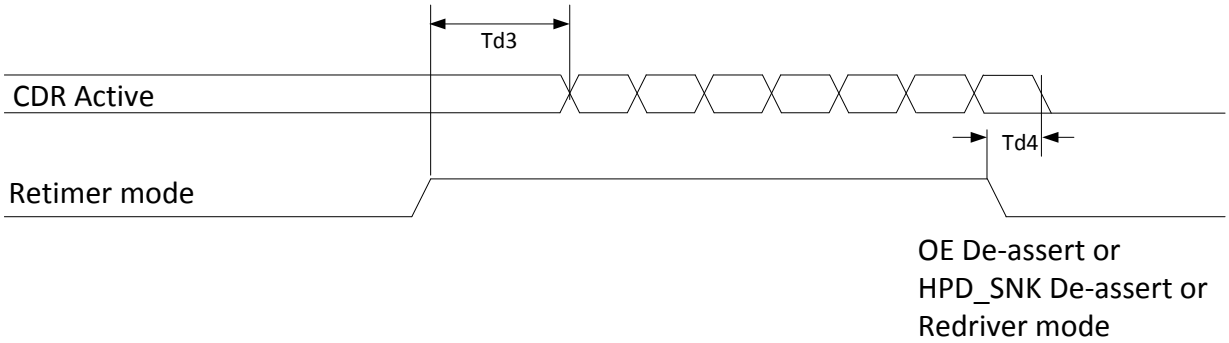

Figure 22. CDR Timing for SNx5DP149

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Feature Description (continued)

Table 1. SNx5DP149 Operation Timing

		MIN	MAX	UNIT
Td1	V_{DD} stable before V_{CC}	0	200	µs
Td2	V_{DD} and V_{CC} stable before OE deassertion	100		µs
Td3	CDR active operation after retimer mode initial		15	ms
Td4	CDR turn off time after retimer mode de-assert		120	ns
VDD_ramp	V_{DD} supply ramp-up requirements	.200	100	ms
VCC_ramp	V_{CC} supply ramp-up requirements	.200	100	ms

8.3.3 Input Lane Swap and Polarity Working

The SNx5DP149 device incorporates the swap function, which can set the input lanes in swap mode. The IN_D2 routes to the OUT_CLK position. The IN_D1 swaps with IN_D0. The swap function only changes the input pins; EQ setup follows new mapping. The user needs to control the register 0x09h bit 7 for SWAP enable. Lane swap is operational in both redriver and retimer mode.

Table 2. Lane Swap(1)

NORMAL OPERATION	SWAP = L OR CSR 0x09h BIT 7 IS 1'b1
IN_D2 → OUT_D2	IN_D2 → OUT_CLK
IN_D1 → OUT_D1	IN_D1 → OUT_D0
IN_D0 → OUT_D0	IN_D2 → OUT_D1
IN_CLK → OUT_CLK	IN_CLK → OUT_D2

(1) The output lanes never change. Only the input lanes change. See and Figure 23.

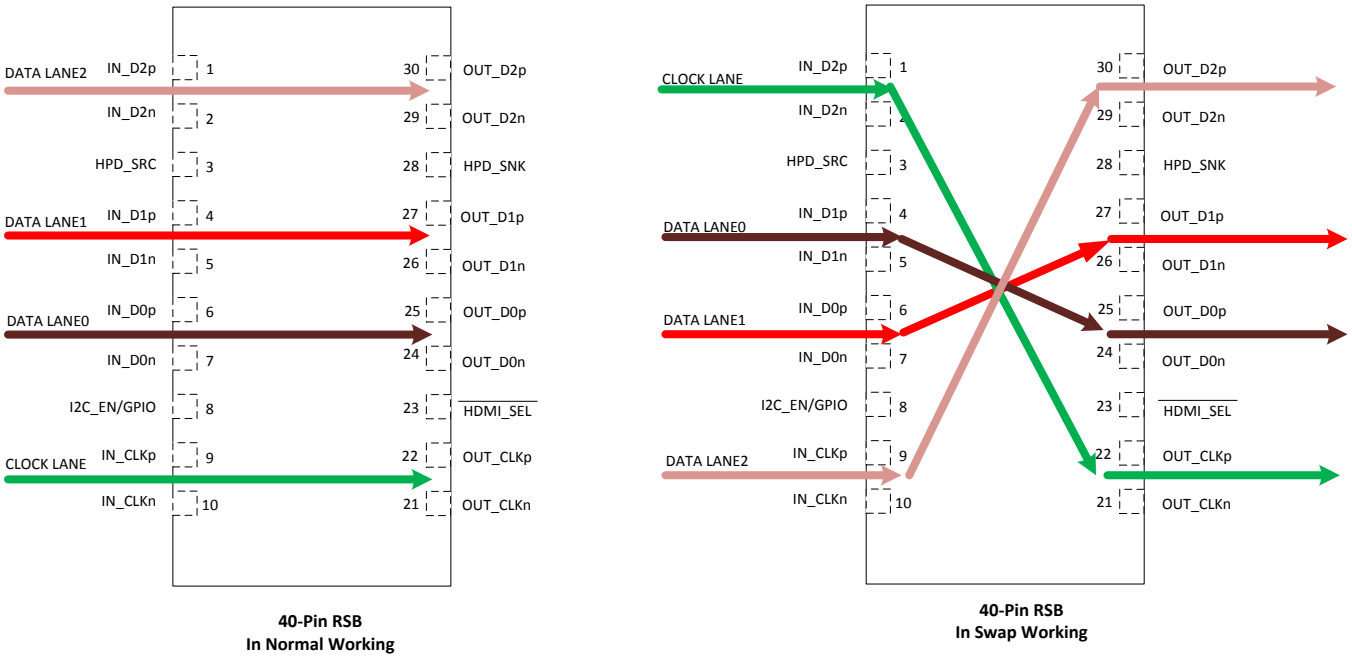

Figure 23. SNx5DP149 Swap Function for 40 Pins

The SNx5DP149 can also change the polarity of the input signals. Use Register 0x9h bit 6 to swap polarity using I^2C. Polarity swap only works for retimer mode. When the device is in automatic redriver to retimer mode this only works when device is in retimer stage. If set and data rate falls below 1.0-Gbps in this mode the polarity function will be lost.

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8.3.4 Main Link Inputs

Standard Dual Mode[1] DisplayPort terminations are integrated on all inputs with expected AC coupling capacitors on board prior to input pins. External terminations are not required. Each input data channel contains an adaptive or fixed equalizer to compensate for cable or board losses. The voltage at the input pins must be limited below the absolute maximum ratings. The input pins have incorporated failsafe circuits. The input pins can be polarity changed through the local I2C register.

8.3.5 Main Link Inputs Debug Tools

There are two methods for debugging a system making sure the inputs to the SNx5DP149 are valid. A TMDS error checker is implemented that will increment an error counter per data lane. This allows the system implementer to determine how the link between the source and SNx5DP149 is performing on all three data lanes. See CSR Bit Field Definitions – RX PATTERN VERIFIER CONTROL/STATUS register in Table 10.

If a high error count is evident, the SNx5DP149 has the ability to provide the general eye quality. A tool is available that uses the I^2C[4] link to download data that can be plotted for an eye diagram. This is available per data lane.

8.3.6 Receiver Equalizer

Equalizers are used to clean up inter-symbol interference (ISI) jitter or loss from the bandwidth-limited board traces or cables. The SNx5DP149 device supports both fixed receiver equalizer (redriver and retimer mode) and adaptive receive equalizer (retimer mode) by setting the EQ_SEL/A0 pin or through I^2C using reg0Ah[5]. When the EQ_SEL/A0 pin is high, the EQ gain is fixed to 14-dB. The EQ gain will be 7.5-dB if the EQ_SEL/A0 pin is set low. The SNx5DP149 device operates in adaptive equalizer mode when EQ_SEL/A0 left floating. Using adaptive equalization the gain will be automatically adjusted based on the data rate to compensate for variable trace or cable loss. Using the local I^2C[4] control, reg0Dh[5:1], the fixed EQ gain can be selected for both data and clock.

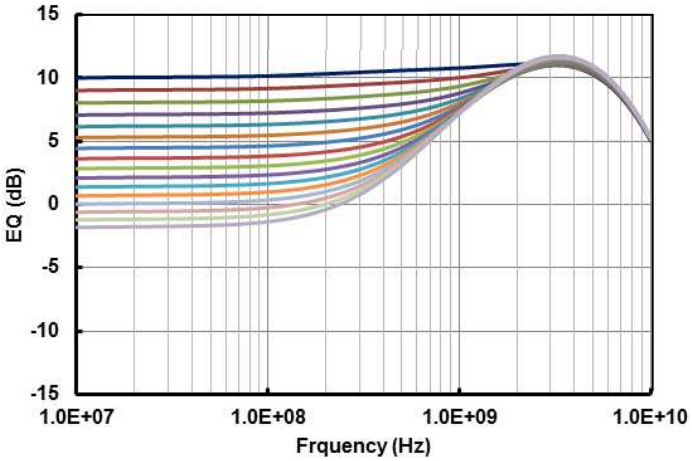

Figure 24. Adaptive EQ Gain Curve

8.3.7 Termination Impedance Control

For HDMI1.4b[2] when data rate over 2 Gbps, the output performance could be better if the termination value between 150 to 300-Ω which was allowed. For compliance this may not be the best solution so be prepared to utilize no termination. The SNx5DP149 supports two different source termination impedances for HDMI1.4b[2] . This can be adjusted by I^2C[4]; reg0Bh[4:3] TX_TERM_CTL.

8.3.8 TMDS Outputs

An 1% precision resistor, 7.06-kΩ, is recommended to be connected from Vsadj pin to ground to allow the differential output swing to comply with TMDS signal levels. The differential output driver provides a typical 10-mA current sink capability when no source term is enabled, which provides a typical 500-mV voltage drop across a 50-Ω termination resistor. As compliance testing is system dependant this resistor value can be adjusted.

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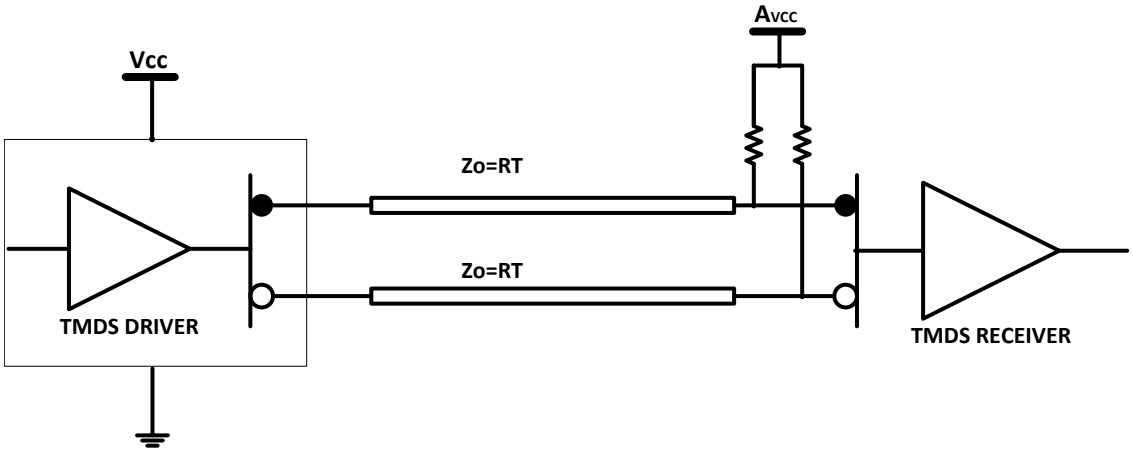

Figure 25. TMDS Driver and Termination Circuit

Referring to Figure 25, if both V_{CC} (device supply) and AVCC (sink termination supply) are powered, the TMDS output signals are high impedance when OE = low. The normal operating condition is that both supplies are active. A total of 33-mW of power is consumed by the terminations independent of the OE logical selection. When AVCC is powered on, normal operation (OE controls output impedance) is resumed. When the power source of the device is off and the power source to termination is on, the IO(off) (output leakage current) specification ensures the leakage current is limited 45-µA or less.

The clock and data lanes V_{OD} can be changed through I^2C[4] (see VSWING_CLK and VSWING_DATA in Table 8 for details). Figure 18 shows the different output voltage based on different Vsadj resistor values.

8.3.8.1 Pre-Emphasis/De-Emphasis

The SNx5DP149 provides De-emphasis as a way to compensate for the ISI loss between the TMDS outputs and the receiver it is driving. There are two methods to implement this function. When in pin strapping mode the PRE_SEL pin controls this. The PRE_SEL pin provides –2-dB, or 0-dB de-emphasis, which allows output signal pre-conditioning to offset interconnect losses from the SNx5DP149 device outputs to a TMDS receiver. TI recommends setting PRE_SEL at 0 dB while connecting to a receiver through a short PCB route. When pulled to ground with a 65-kΩ resistor –2-dB can be realized, see Figure 6. When using I^2C, Reg0Ch[1:0] is used to make these adjustments.

As there are times true pre-emphasis may be the best solution there are two ways to accomplish this. If pin strapping is being use the best method is to reduce the Vsadj resistor value increasing the V_{OD} and then pulling the PRE_SEL pin to ground using the 65-kΩ resistor, see Figure 26. If using I^2C this can be accomplished using two methods. First is similar to pin strapping by adjusting the Vsadj resistor value and then implementing –2-dB de-emphasis. Second method is to set Reg0Ch[7:5] = 011 and the set Reg0Ch[1:0] = 01 which accomplishes the same pre-emphasis setting. See Figure 27.

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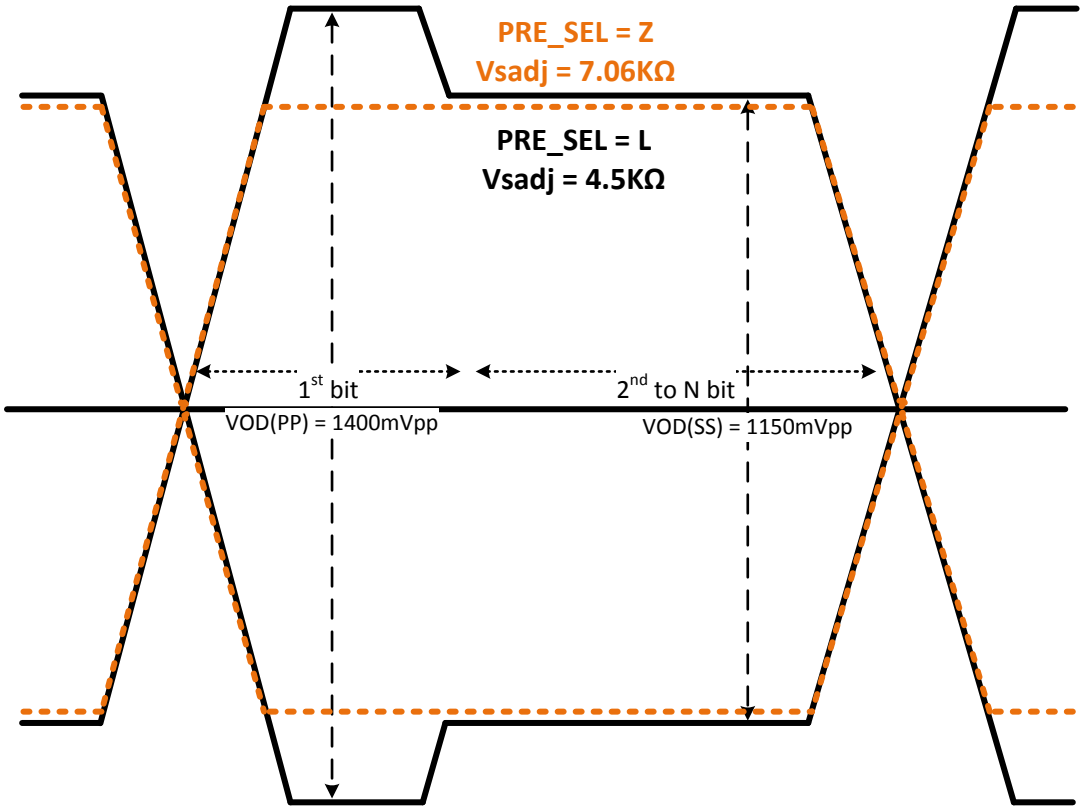

Figure 26. Pre-Emphasis Using Pin Strapping Method

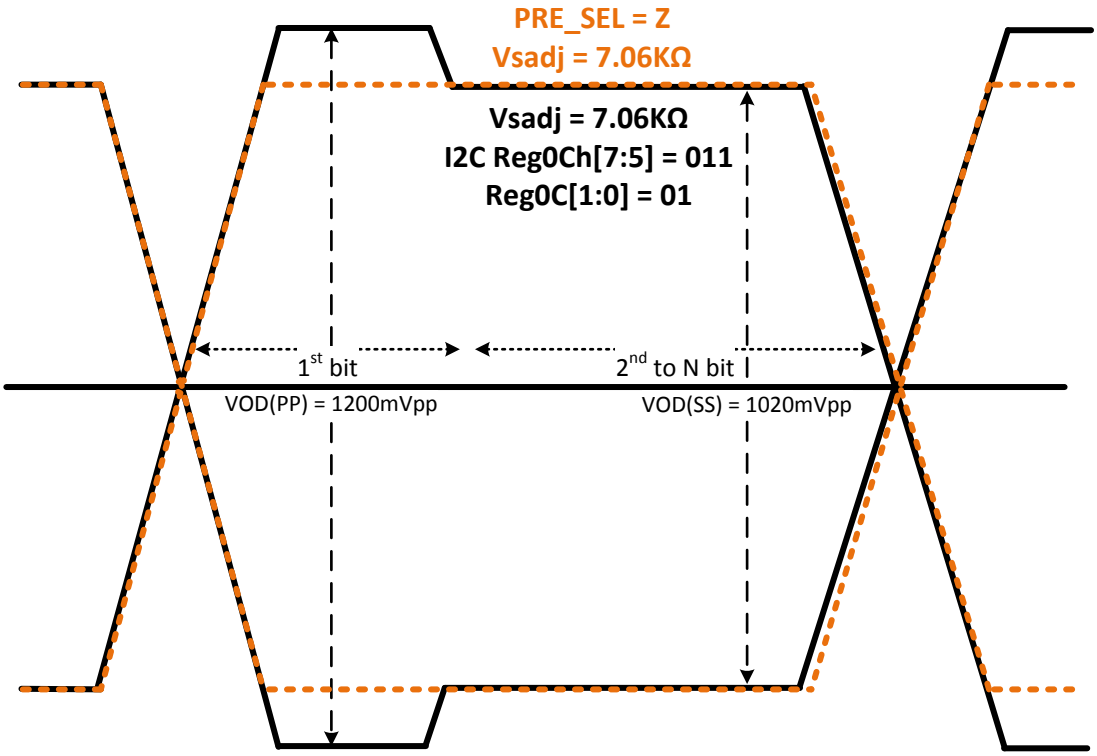

Figure 27. Pre-Emphasis Using I^2C Method

8.4 Device Functional Modes

8.4.1 Retimer Mode

Clock and data recovery circuits (CDR) are used to track, sample and retime the equalized data bit streams. The CDRs are designed with loop bandwidth to minimize the amount of jitter transfer from the video source to the TMDS outputs. Input jitter within the CDR's PLL bandwidth, < 1-MHz, will be transferred to the TMDS outputs. Higher frequency jitter above the CDR loop bandwidth is attenuated, providing a jitter cleaning function to reduce the amount of high frequency jitter from the video source. The retimer is automatically activated at pixel clock above approximately 100-MHz when jitter cleaning is needed for robust operation. The retimer operates at about 1.0 to 3.4-Gbps DR supporting HDMI1.4b[3]. At pixel clock frequency below about 100 MHz, the SNx5DP149 automatically bypasses the internal retimer and operates as a redriver. When the video source changes resolution, the internal retimer starts the acquisition process to determine the input clock frequency and acquire lock to the new data bit streams. During the clock frequency detection period and the retimer acquisition period (that last approximately 7-ms), the TMDS drivers can be kept active (default) or programmed to be disabled to avoid sending invalid clock or data to the downstream receiver.

8.4.2 Redriver Mode

The SNx5DP149 also has a redriver mode that can be enabled through I^2C[4]; at offset address 0Ah bits 1:0 DEV_FUNC_MODE. When in this mode, the CDR and PLL are shut off, thus reducing power. Jitter performance is degraded as the device will now only compensate for ISI loss in the link. In redriver mode HDMI1.4b[3] compliance is not guaranteed as skew compensation and retiming functions are disabled. Excessive random or phase jitter will not be compensated.

8.4.3 DDC Functional Description

The SNx5DP149 solves sink- or source-level issues by implementing a master/slave control mode for the DDC bus. When the SNx5DP149 detects the start condition on the DDC bus from the SDA_SRC/SCL_SRC, it will transfer the data or clock signal to the SDA_SNK/SCL_SNK with little propagation delay. When SDA_SNK detects the feedback from the downstream device, the SNx5DP149 will pull up or pull down the SDA_SRC bus and deliver the signal to the source.

The DDC link defaults to 100 kbps, but can be set to various values including 400 kbps by setting the correct value to address 22h (see Table 3) through the I^2C interface. The DDC lines are 5-V tolerant. The HPD_SRC goes to high impedance when VCC is under low power conditions, < 1.5-V.

8.5 Register Maps

8.5.1 DP-HDMI Adaptor ID Buffer

The SNx5DP149 device includes the DP-HDMI adapter ID buffer for HDMI/DVI adaptor recognition, defined by the VESA DisplayPort Dual-Mode Standard Version 1.1, accessible by standard I^2C[4] protocols through the DDC interface when the HDMI_SEL/A1 pin is low. The DP-HDMI adapter buffer and extended DDC register for Type 2 capability is accessed at target addresses 80h (Write) and 81h (Read).

The DP-HDMI adapter buffer contains a read-only phrase DP-HDMI ADAPTOR<EOT> converted to ASCII characters, as shown in Table 3, and supports the WRITE command procedures (accessed at target address 80h) to select the subaddress, as recommended in the VESA DisplayPort Interoperability Guideline Adaptor Checklist Version 1.0 section 2.3.

Table 3. SNx5DP149 DP-HDMI Adaptor ID Buffer and Extended DDC

Address	Description	Value HDMI	Value DVI	Read or Read/Write
00h	HDMI ID code	44h	00h	Read only
01h		50h	00h	
02h		2Dh	00h	
03h		48h	00h	
04h		44h	00h	
05h		4Dh	00h	
06h		49h	00h	
07h		20h	00h	
08h		41h	00h	
09h		44h	00h	
0Ah		41h	00h	
0Bh		50h	00h	
0Ch		54h	00h	
0Dh		4Fh	00h	
0Eh		52h	00h	
0Fh		04h	00h	
10h	Video Adaptor Identifier Bit 2:0 ADAPTOR_REVISION	0	0	Read only
	Bit 3 Reserved: but 0 for type 2	0	0	
	Bits 7:4 1010 = Dual mode defined by dual mode[1] standard	1010	0	
11h	IEE_OUI first two hex digits	08h	08h	Read only
12h	IEE_OUI second two hex digits	00h	00h	Read only
13h	IEE_OUI third two hex digits	28h	28h	Read only
14h	Device ID	44h	44h	Read only
15h		50h	50h	
16h		31h	31h	
17h		34h	34h	
18h		39h	39h	
19h		00h	00h	
1Ah	Hardware revision	00h	00h	Read only
	Bits 7:4 major revision			
	Bits 3:0 minor revision			
1Bh	Firmware or software major revision	00h	00h	Read only
1Ch	Firmware or software minor revision	00h	00h	Read only

Register Maps (continued)

Table 3. SNx5DP149 DP-HDMI Adaptor ID Buffer and Extended DDC (continued)

Address	Description	Value HDMI	Value DVI	Read or Read/Write
1Dh	Max TMDS clock rate Default value is 88h in HDMI column Note: Value determined by taking clock rate and dividing by 2.5 and converting to HEX. For HDMI2.0 extend as if the clock rate extended instead of its actual method, clock 1/10 DR and not 1/40 DR.	88h	42h	Read only
1Eh	If I2C_DR_CTL = 0 the value is 0Fh → If DDC_AUX_DR_SEL = 0 the value is 0Fh If I2C_DR_CTL = 1 the value is 1Fh → If DDC_AUX_DR_SEL = 1 then value is 1Fh If I2C_DR_CTL = 0 the value is 0Fh If I2C_DR_CTL = 1 the value is 1Fh	0Fh	0Fh	Read only
1Fh	Reserved	00h	00h	Write/Read
20h	$\overline{\text{TMDS\_OE}}$ Bit 0: 0 = TMDS_ENABLED (default) 1 = TMDS_DISABLED Bits 7:1 Reserved	00h	00h	Write/Read
21h	HDMI Pin Control Bit 0 = CEC_EN Enables connection between the HDMI CEC pin connected to the sink and the CONFIG2 pin to the upstream device + 27-kΩ pullup. 0 = CEC_ DISABLED (default) 1 = CEC_ ENABLED Bits 7:1 = RESERVED	00h	00h	Write/Read
22h	Writing a bit pattern to this register that is not defined above may result in an unpredictable I^2C speed selection, but the adaptor must continue to otherwise work normally. Only applicable when using I^2C-over-AUX transport 01h = 1-Kbps 02h = 5-Kbps 04h = 10-Kbps 08h = 100-kbps 10h = 400-Kbps (RSVD in Dual Mode STND) On read, the dual-mode cable adaptor returns a value to indicate the speed currently in use. The default I2C speed prior to software writing to this register is 100-Kbps. Illegal write value shall write register default (08h). This register sets the DDC output DR whether I^2C-over-AUX or straight DDC	08h	08h	Write/Read
23h-FFh	Reserved	00h	00h	Read

8.5.2 Local I^2C Interface Overview

The SCL_CTL and SDA_CTL pins are used for I^2C clock and I^2C data respectively. The SNx5DP149 I^2C interface conforms to the 2-wire serial interface defined by the I^2C Bus Specification, Version 2.1 (January 2000), and supports the fast mode transfer up to 400 kbps.

The device address byte is the first byte received following the start condition from the master device. The 7-bit device address for the SNx5DP149 device decides by the combination of EQ_SEL/A0 and $\overline{\text{HDMI\_SEL}}$/A1. Table 4 clarifies the SNx5DP149 device target address.

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Table 4. I²C Device Address Description

A1/A0	SNx5DP149 I²C Device Address								ADD
	7 (MSB)	6	5	4	3	2	1	0 (W/R)	
00	1	0	1	1	1	1	0	0/1	BC/BD
01	1	0	1	1	1	0	1	0/1	BA/BB
10	1	0	1	1	1	0	0	0/1	B8/B9
11	1	0	1	1	0	1	1	0/1	B6/B7

8.5.3 I²C Control Behavior

Follow this procedure to write to the SNx5DP149 device I²C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the SNx5DP149 device 7-bit address and a zero-value W/R bit to indicate a write cycle.
2. The SNx5DP149 device acknowledges the address cycle by combination of A0 and A1.
3. The master presents the subaddress (I²C register within SNx5DP149 device) to be written, consisting of one byte of data, MSB-first.
4. The SNx5DP149 device acknowledges the subaddress cycle.
5. The master presents the first byte of data to be written to the I²C register.
6. The SNx5DP149 device acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the SNx5DP149.
8. The master terminates the write operation by generating a stop condition (P).

Follow this procedure to read the SNx5DP149 I²C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the SNx5DP149 7-bit address and a one-value W/R bit to indicate a read cycle.
2. The SNx5DP149 device acknowledges the address cycle.
3. The SNx5DP149 device transmit the contents of the memory registers MSB-first starting at register 00h.
4. The SNx5DP149 device will wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I²C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the SNx5DP149 device transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

NOTE

No sub-addressing is included for the read procedure, and reads start at register offset 00h and continue byte by byte through the registers until the I²C master terminates the read operation.

Refer to Table 6 for the SNx5DP149 device local I²C register descriptions. Reads from reserved fields return 0s and writes are ignored.

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8.5.4 I²C Control and Status Registers

Reads from reserved fields return 0, and writes to read-only reserved registers are ignored. Writes to reserved registers, which are marked with 'W', produce unexpected behavior. All addresses not defined by this specification are considered reserved. Reads from these addresses return 0 and writes will be ignored.

8.5.4.1 Bit Access Tag Conventions

A table of bit descriptions is typically included for each register description that indicates the bit field name, field description, and the field access tags. The field access tags are described in Table 5.

Table 5. Field Access Tags

ACCESS TAG	NAME	DESCRIPTION
R	Read	The field is read by software
W	Write	The field is written by software
S	Set	The field is set by a write of one. Writes of 0 to the field have no effect
C	Clear	The field is cleared by a write of 1. Writes of 0 to the field have no effect
U	Update	Hardware may autonomously update this field
NA	No access	Not accessible or not applicable

8.5.4.2 CSR Bit Field Definitions

8.5.4.2.1 ID Registers

Table 6. ID Registers

ADDRESS	BIT	DESCRIPTION	ACCESS
00h:07h	7:0	DEVICE_ID These fields return a string of ASCII characters "DP149" followed by three space characters. Address 0x00 – 0x07 = {0x44"D", 0x50"P", 0x31"1", 0x34"4", 0x39"9", 0x20, 0x20, 0x20}	R
08h	7:0	REV _ID. This field identifies the device revision. 0000001 – DP149 revision 1	R

8.5.4.2.2 Misc Control

Table 7. Misc Control

ADDRESS	BIT	DEFAULT	DESCRIPTION	ACCESS
09h	7	1'b0	SWAP_EN: This field enables swapping the input main link lanes **0 – Disable (default)** 1 – Enable Note: field is loaded from SWAP/POL pin; Writes ignored when I2C_EN/PIN = 0	RWU
	6	1'b0	LANE_POLARITY: swaps the input data and clock lanes polarity. **0 – Disabled: No polarity swap** 1 – Swaps the input data and clock lane polarity Note: field is loaded from SWAP/POL pin; Writes ignored when I2C_EN/PIN = 0. This feature is only valid when in retimer mode.	RWU
	5:4	2'b00	Reserved	R
	3	1'b0	PD_EN **0 – Normal working (default)** 1 – Forced power-down by I²C, lowest power state	RW
	2	1'b0	HPD_AUTO_PWRDWN_DISABLE **0 – Automatically enters power down mode based on HPD_SNK (default)** 1 – Will not automatically enter power mode based upon HPD_SNK	RW
	1:0	2'b10	I2C_DR_CTL. I2C data rate supported for configuring device 00 – 5-kbps 01 – 10-kbps **10 – 100-kbps (default)** 11 – 400-kbps	RW

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Table 7. Misc Control (continued)

ADDRESS	BIT	DEFAULT	DESCRIPTION	ACCESS
0Ah	7	1'b0	Application Mode Selection **0 – Source (default) - Set the adaptive EQ mid point to between 6.5-dB and 7.5-dB** 1 – Sink - Sets the adaptive EQ starting point to between 12-dB and 13-dB	RW
	6	1'b0	HPDSNK_GATE_EN: This field sets the functional relationship between HPD_SNK and HPD_SRC. **0 – HPD_SNK passed through to the HPD_SRC (default)** 1 – HPD_SNK will not pass through to the HPD_SRC.	RW
	5	1'b1	EQ_ADA_EN: this field enables the equalizer working state. 0 – Fixed EQ **1 – Adaptive EQ (default)** Writes are ignored when I2C_EN/PIN = 0	RWU
	4	1'b1	EQ_EN: this field enables the receiver equalizer. 0 – EQ disabled **1 – EQ enable (default)**	RW
	3	1'b0	Reserved	RW
	2	1'b0	APPLY_RXTX_CHANGES , Self clearing write-only bit. Writing a 1 to this bit will apply new slew, tx_term, twpst1, eqen, eqadapten, swing, eqftc, eqlev settings to the clock and data lanes. Writes to the respective registers do not take immediate effect. This bit does not need to be written if I^2C configuration occurs while OE or hpd_sink are low, I^2C power down is active.	W
	1:0	2'b01	DEV_FUNC_MODE: This field selects the device working function mode. 00 – Redriver mode across full range 250 Mbps to 3.4-Gbps **01 - Automatic redriver to retimer crossover at 1.0 Gbps (default)** 10 - Reserved 11 - Retimer mode across full range 250 Mbps to 3.4-Gbps When moving between the different modes, the device needs to toggle the power setting from 1 to 0, then back to 1, for proper initializing of the crossover mode.	RW

Mode Selection Definition: This bit lets the receiver know where the device is located in a system for the purpose of centering the AEQ point. The SNx5DP149 is targeting the source application, so the default value is 0, which will center the EQ at 6.5 to 7.5-dB , see Table 9. If the SNx5DP149 is in a dock or sink application, the value should be changed to a value of 1, which will center the EQ at 12 to 13-dB .

8.5.4.2.3 HDMI Control

Table 8. HDMI Control

ADDRESS	BIT	DEFAULT	DESCRIPTION	ACCESS
0Bh	7:6	2'b00	SLEW_CTL. Slew rate control.2'00 is fastest and 2'b11 is slowest Writes ignored when I2C_EN/PIN = 0	RWU
	5	1'b0	HDMI_SEL: Contro; Writes ignored when I2C_EN/PIN = 0l **0 – HDMI (default)** 1 – DVI	RWU
	4:3	2'b00	TX_TERM_CTL: Controls termination for HDMI TX **00 – No termination** 01 – 150 to 300-Ω 10 – Reserved 11 – 75 to 150-Ω	RWU
	2	1'b0	Reserved	R
	1	1'b0	. Reserved	R
	0	1'b0	Reserved	R

Table 8. HDMI Control (continued)

ADDRESS	BIT	DEFAULT	DESCRIPTION	ACCESS
0Ch	7:5	3'b000	VSWING_DATA: Data output swing control **000 – Vsadj set** 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7%	RW
	4:2	3'b000	VSWING_CLK: Clock Output Swing Control **000 – Vsadj set** 001 – Increase by 7% 010 – Increase by 14% 011 – Increase by 21% 100 – Decrease by 30% 101 – Decrease by 21% 110 – Decrease by 14% 111 – Decrease by 7% Note: Default is set by DR, which means standard based swing values but this allows for the swing to be overridden by selecting one of these values	RW
	1:0	2'b00	HDMI_TWPST1. HDMI de-emphasis FIR post-cursor-1 signed tap weight. **00 – No de-emphasis** 01 – 2-dB de-emphasis 10 – Reserved 11 – Reserved	RWU

8.5.4.2.4 Equalization Control Register

Table 9. Equalization Control Register

ADDRESS	BIT	DEFAULT	DESCRIPTION	ACCESS
0Dh	7:6	2'b00	Reserved	RW
	5:3	1'b000	**Data Lane EQ – Sets fixed EQ values** HDMI1.4b[2] **000 – 0-dB** 001 – 4.5-dB 010 – 6.5-dB 011 – 8.5-dB 100 – 10.5-dB 101 – 12-dB 110 – 14-dB 111 – 16.5-dB	RW
	2:1	1'b00	**Clock Lane EQ - Sets fixed EQ values** HDMI1.4b[2] **00 – 0-dB** 01 – 1.5-dB 10 – 3-dB 11 – RSVD	RW
	0	1'b0	Reserved	RW

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8.5.4.2.5 EyeScan Control Register

Table 10. EyeScan Control Register

ADDRESS	BITS	DEFAULT	DESCRIPTION	ACCESS
0Eh	7:4	4'b0000	PV_SYNC[3:0]. Pattern timing pulse. This field is updated for 8UI once every cycle of the PRBS generator. 1 bit per lane.	R
	3:0	4'b0000	PV_LD[3:0]. Load pattern-verifier controls into RX lanes. When asserted high, the PV_TO, PV_SEL, PV_LEN, PV_CP20, and PV_CP values are enabled into the corresponding RX lane. These values are then latched and held when PV_LD[n] is subsequently de-asserted low. 1 bit per lane.	RWU
0Fh	7:4	4'b0000	PV_FAIL[3:0]. Pattern verification mismatch detected. 1 bit per lane.	RU
	3:0	4'b0000	PV_TIP[3:0]. Pattern search/training in progress. 1 bit per lane.	RU
10h	7	1'b0	PV_CP20. Customer pattern length 20 or 16 bits. **0 – 16 bits** 1 – 20 bits	RW
	6	1'b0	Reserved	R
	5:3	3'b000	PV_LEN[2:0]. PRBS pattern length **000 – PRBS7** 001 – PRBS11 010 – PRBS23 011 – PRBS31 100 – PRBS15 101 – PRBS15 110 – PRBS20 111 – PRBS20	RW
	2:0	3'b000	PV_SEL[24:0]. Pattern select control **000 – Disabled** 001 – PRBS 010 – Clock 011 – Custom 1xx – Timing only mode with sync pulse spacing defined by PV_LEN	RW
11h	7:0	'h00	PV_CP[7:0]. Custom pattern data.	RW
12h	7:0	'h00	PV_CP[15:8]. Custom pattern data.	RW
13h	7:4	4'b0000	Reserved	R
	3:0	4'b0000	PV_CP[19:16]. Custom pattern data. Used when PV_CP20 = 1'b1.	RW
14h	7:3	5'b00000	Reserved	R
	2:0	3'b000	PV_THR[2:0]. Pattern-verifier retain threshold.	RW
15h	7	1'b0	DESKEW_CMPLT: Indicates TMDS lane deskew has completed when high	R
	6:5	2'b00	Reserved	R
	4	1'b0	BERT_CLR. Clear BERT counter (on rising edge).	RSU
	3	1'b0	TST_INTQ_CLR. Clear latched interrupt flag.	RSU
	2:0	3'b000	TST_SEL[2:0]. Test interrupt source select.	RW
16h	7:4	4'b0000	PV_DP_EN[3:0]. Enabled datapath verified based on DP_TST_SEL, 1 bit per lane.	RW
	3	1'b0	Reserved	R
	2:0	3'b000	DP_TST_SEL[2:0] Selects pattern reported by BERT_CNT[11:0], TST_INT[0] and TST_INTQ[0]. PV_DP_EN is non-zero **000 – TMDS disparity or data errors** 001 – FIFO errors 010 – FIFO overflow errors 011 – FIFO underflow errors 100 – TMDS deskew status 101 – Reserved 110 – Reserved 111 – Reserved	RW
17h	7:4	4'b0000	TST_INTQ[3:0]. Latched interrupt flag. 1 bit per lane	RU
	3:0	4'b0000	TST_INT[3:0]. Test interrupt flag. 1 bit per lane.	RU
18h	7:0	'h00	BERT_CNT[7:0]. BERT error count. Lane 0	RU

Table 10. EyeScan Control Register (continued)

ADDRESS	BITS	DEFAULT	DESCRIPTION	ACCESS
19h	7:4	4'b0000	Reserved	R
	3:0	4'b0000	BERT_CNT[11:8]. BERT error count. Lane 0	RU
1Ah	7:0	'h00	BERT_CNT[19:12]. BERT error count. Lane 1	RU
1Bh	7:4	4'b0000	Reserved	R
	3:0	4'b0000	BERT_CNT[23:20]. BERT error count. Lane 1	RU
1Ch	7:0	'h00	BERT_CNT[31:24]. BERT error count. Lane 2	RU
1Dh	7:4	4'b0000	Reserved	R
	3:0	4'b0000	BERT_CNT[35:32]. BERT error count. Lane 2	RU
1Eh	7:0	'h00	BERT_CNT[19:12]. BERT error count. Lane 3	RU
1Fh	7:4	4'b0000	Reserved	R
	3:0	'h00	BERT_CNT[23:20]. BERT error count. Lane 3	RU
20h	7	1'b0	Power Down Status Bit **0 – Normal Operation** 1 – Device in Power Down Mode	R
	6	1'b0	Standby Status Bit **0 – Normal Operation** 1 – Device in Standby Mode	R
	5:0	6'b000000	Reserved	R

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Use Case of SNx5DP149

SNx5DP149 can be used on the motherboard and dongle applications. The following use case diagrams show the connection of DDC between source side and sink side. The control pin pull up and pull down resistors are shown from reference. If a high is needed only use the pull up. If a low is needed only use the pull down. If mid level is to be selected do not use either resistors and leave the pin floating/No connect. The 6.5-KΩ Vsadj resistor value shown is explained further in the compliance section.

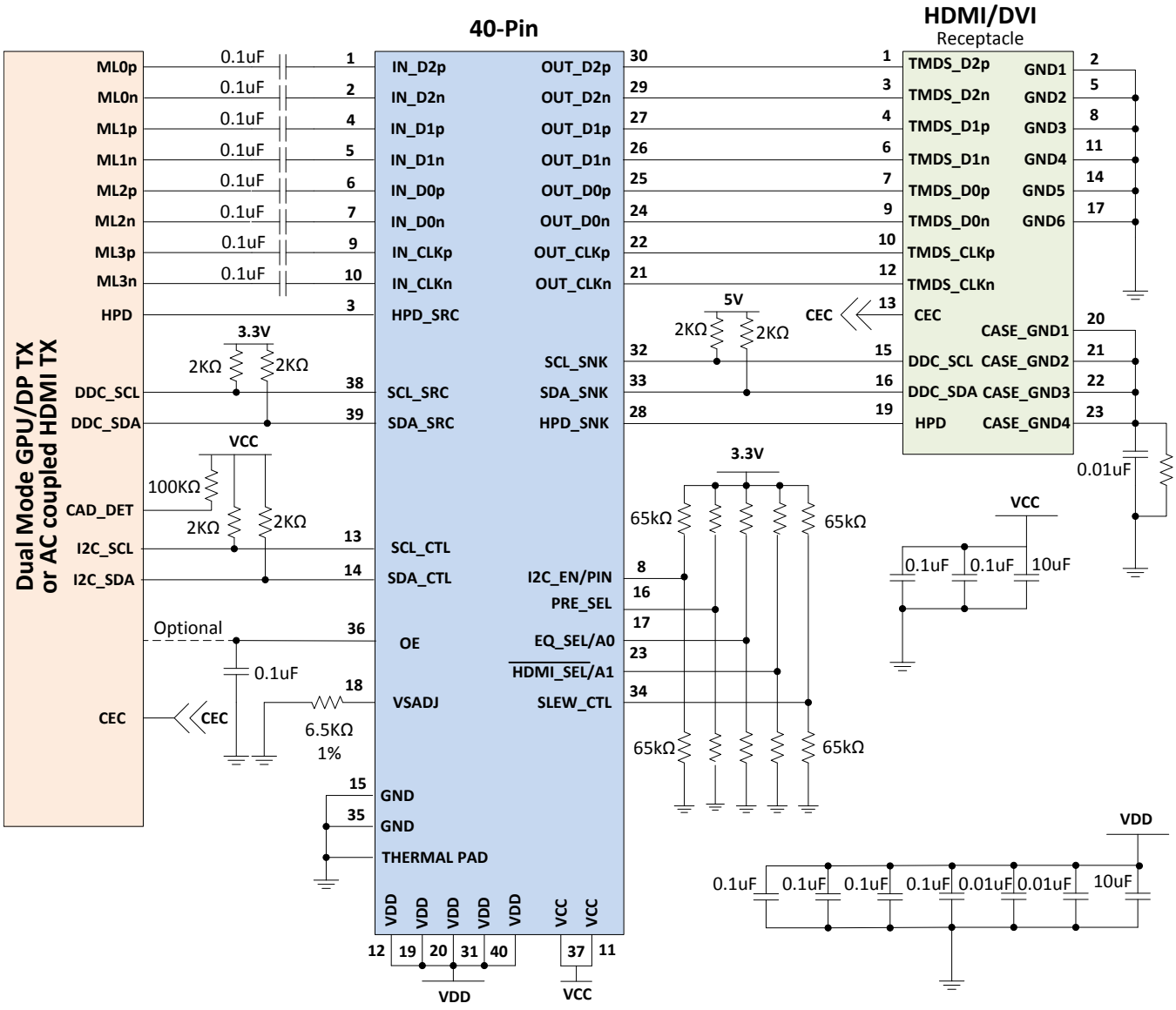

Figure 28. Implementation for Motherboard

Application Information (continued)

Figure 28 shows the original connection of SNx5DP149 on motherboard through the DDC channel. The DDC DR default is 100-kHz and is capable to adjust to 400-kHz.

shows the SNx5DP149 in the dongle application. It uses the unified structure on DisplayPort connector.

9.1.2 DDC Pullup Resistors

NOTE

This section is for information only and subject to change depending upon system implementation.

The pullup resistor value is determined by two requirements:

1. The maximum sink current of the I^2C buffer:

   The maximum sink current is 3-mA or slightly higher for an I^2C driver supporting standard-mode I^2C[4] operation.

$$R_{up(min)} = \frac{VCC}{Isink} \quad (1)$$

2. The maximum transition time on the bus:

   The maximum transition time, T, of an I^2C bus is set by an RC time constant, where R is the pullup resistor value, and C is the total load capacitance. The parameter, k, can be calculated from Equation 3 by solving for t, the times at which certain voltage thresholds are reached. Different input threshold combinations introduce different values of t. Table 11 summarizes the possible values of k under different threshold combinations.

$$T = k \times RC \quad (2)$$

$$V(t) = VCC \times \left(1 - e^{\frac{-t}{RC}}\right) \quad (3)$$

Table 11. Value k Upon Different Input Threshold Voltages

V_{th-}|V_{th+}	0.7 V_{CC}	0.65 V_{CC}	0.6 V_{CC}	0.55 V_{CC}	0.5 V_{CC}	0.45 V_{CC}	0.4 V_{CC}	0.35 V_{CC}	0.3 V_{CC}
0.1 VCC	1.0986	0.9445	0.8109	0.6931	0.5878	0.4925	0.4055	0.3254	0.2513
0.15 VCC	1.0415	0.8873	0.7538	0.6360	0.5306	0.4353	0.3483	0.2683	0.1942
0.2 VCC	0.9808	0.8267	0.6931	0.5754	0.4700	0.3747	0.2877	0.2076	0.1335
0.25 VCC	0.9163	0.7621	0.6286	0.5108	0.4055	0.3102	0.2231	0.1431	0.0690
0.3 VCC	0.8473	0.6931	0.5596	0.4418	0.3365	0.2412	0.1542	0.0741	

From Equation 1, $R_{up(min)}$ = 5.5-V / 3-mA = 1.83-kΩ to operate the bus under a 5-V pullup voltage and provide less than 3-mA when the I^2C device is driving the bus to a low state. If a higher sink current, for example 4 mA, is allowed, $R_{up(min)}$ can be as low as 1.375-kΩ.

If DDC is working at a standard mode of 100-Kbps, the maximum transition time, T, is fixed, 1 µs, and using the k values from Table 11, the recommended maximum total resistance of the pullup resistors on an I^2C bus can be calculated for different system setups. If DDC is working in a fast mode of 400-kbps, the transition time should be set at 300 ns, according to I^2C[4] specification.

To support the maximum load capacitance specified in the HDMI specification, $C_{cable(max)}$ = 700-pF, C_{source} = 50-pF, C_i = 50-pF, and $R_{(max)}$ can be calculated as shown in Table 12.

Table 12. Pullup Resistor Upon Different Threshold Voltages and 800-pF Loads

V_{th-}|V_{th+}	0.7 V_{CC}	0.65 V_{CC}	0.6 V_{CC}	0.55 V_{CC}	0.5 V_{CC}	0.45 V_{CC}	0.4 V_{CC}	0.35 V_{CC}	0.3 V_{CC}	UNIT
0.1 VCC	1.14	1.32	1.54	1.8	2.13	2.54	3.08	3.84	4.97	kΩ
0.15 VCC	1.2	1.41	1.66	1.97	2.36	2.87	3.59	4.66	6.44	kΩ
0.2 VCC	1.27	1.51	1.8	2.17	2.66	3.34	4.35	6.02	9.36	kΩ

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Table 12. Pullup Resistor Upon Different Threshold Voltages and 800-pF Loads (continued)

V_{th-}/V_{th+}	0.7 V_{CC}	0.65 V_{CC}	0.6 V_{CC}	0.55 V_{CC}	0.5 V_{CC}	0.45 V_{CC}	0.4 V_{CC}	0.35 V_{CC}	0.3 V_{CC}	UNIT
0.25 VCC	1.36	1.64	1.99	2.45	3.08	4.03	5.6	8.74	18.12	kΩ
0.3 VCC	1.48	1.8	2.23	2.83	3.72	5.18	8.11	16.87	—	kΩ

To accommodate the 3-mA drive current specification, a narrower threshold voltage range is required to support a maximum 800-pF load capacitance for a standard-mode I^2C bus.

9.2 Typical Application

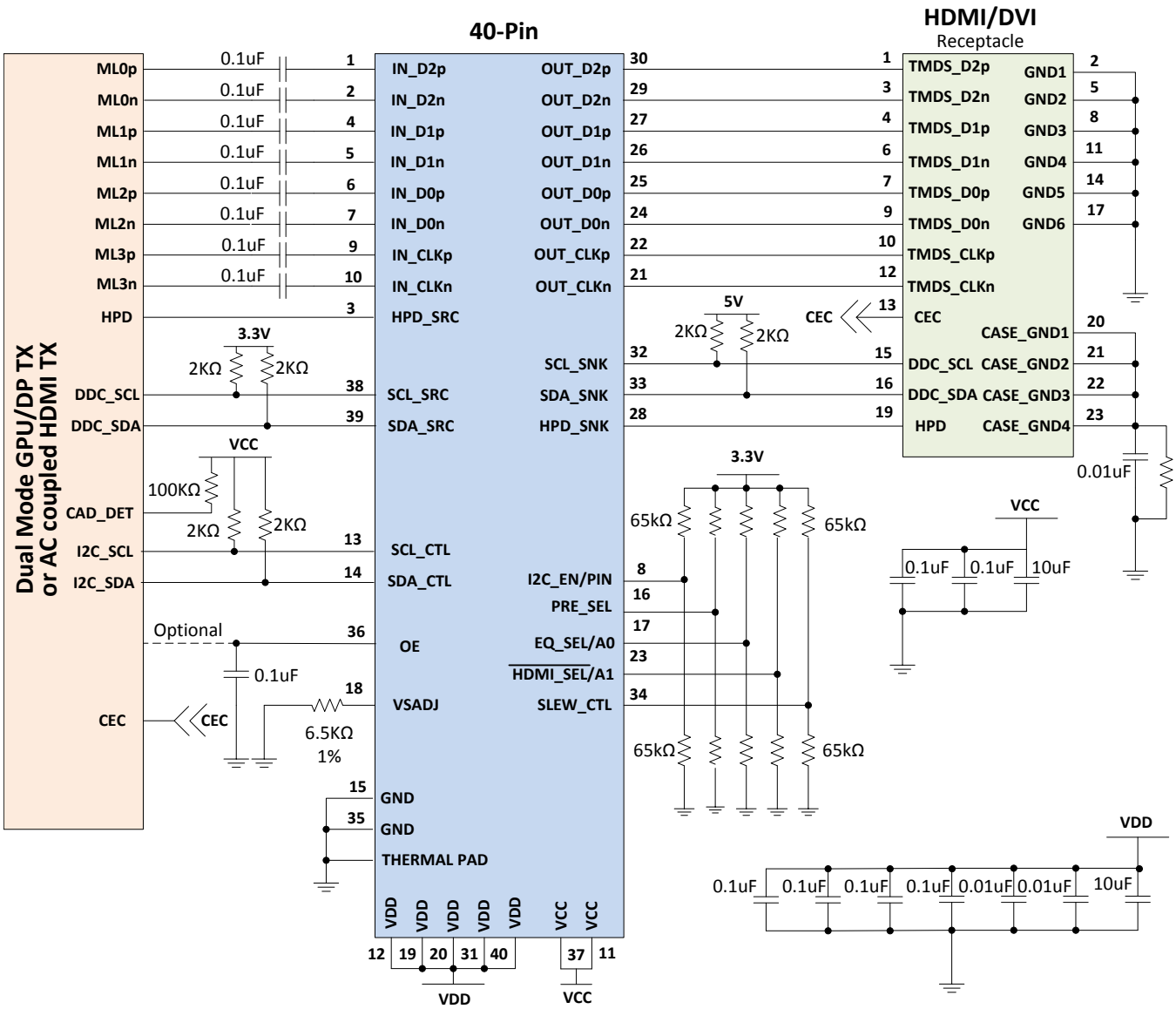

Figure 29. Implementation for Motherboard Schematic

Typical Application (continued)

9.2.1 Design Requirements

The SNx5DP149 can be designed into many types of applications. All applications have certain requirements for the system to work properly. Two voltage rails are required to support the lowest possible power consumption. The OE pin must have a 0.1-µF capacitor to ground. This pin can be driven by a processor but the pin needs to change states after voltage rails have stabilized. Configure the device by using I^2C. Pin strapping is provided as I^2C is not available in all cases. Because sources may have different naming conventions, confirm the link between the source and the SNx5DP149 is correctly mapped. A swap function is provided for the input pins in case signaling is reversed between the source and the device. For the control pins the values provided below are when they are being controlled by a micro-controller. If this is not the case then using the 65-kΩ for a pull up for high, pulled down for low, and left floating for mid level.

Table 13. Design Parameters

DESIGN PARAMETER	VALUE
V_{CC}	3.3 V
V_{DD}	1.1 V
Main link input voltage	V_{ID} = 75 mVpp to 1.2 Vpp
Control pin Low	65-kΩ pulled to GND
Control pin Mid	No Connect
Control pin High	65-kΩ pulled to 3.3-V
Vsadj resistor	7.06-kΩ
Main link AC decoupling capacitor	75 to 200 nF, recommend 100 nF

9.2.2 Detailed Design Procedure

The SNx5DP149 is a signal conditioner that provides AC coupling to DC coupling level shifting, to support Dual Mode DisplayPort-capable GPUs or GPUs with AC-coupled drive capability to support HDMI or DVI connectors and compliance. Signal conditioning is accomplished using receive equalization, retiming, and output driver configurability. The transmitter drives 2 to 3 inches of board trace and connector.

Designing in the SNx5DP149 requires the following:

- Determine the loss profile between the GPU and the HDMI/DVI connector.
- Based upon the loss profile and signal swing, determine the optimal location for the SNx5DP149, to pass electrical compliance.
- Use the typical application drawings in *Use Case of SNx5DP149* for information on using the AC coupling capacitors and control pin resistors.
- The DP149 has a receiver adaptive equalizer by default but can also be configured for fixed value equalization using the EQ_SEL control pin.
- Set the VOD, pre-emphasis, termination, and edge rate levels to support compliance by using the appropriate Vsadj resistor value and by setting the PRE_SEL and SLEW_CTL control pins.
- The thermal pad must be connected to ground.
- See the schematics in *Application Information* on recommended decouple capacitors from VCC pins to ground.

PRODUCT PREVIEW

9.2.3 Application Curves

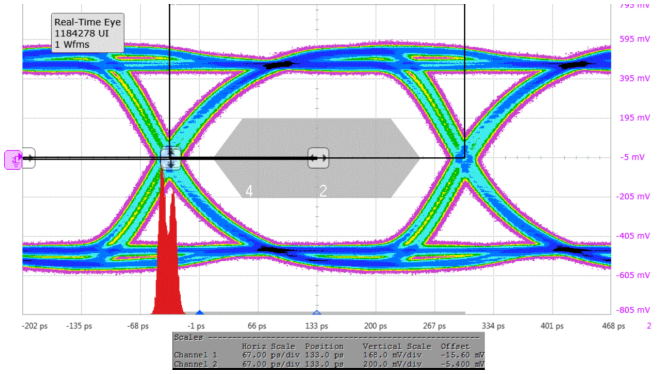

Figure 30. 4k2k30 TX Compliance Eye

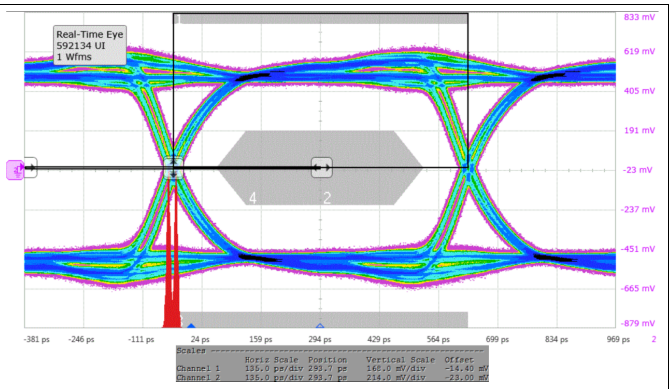

Figure 31. 1080p TX Compliance Eye

9.3 System Example

9.3.1 Compliance Testing

Compliance testing is very system design specific. Properly designing the system and configuring the SNx5DP149 can help pass transmitter compliance for the system. The following information is the starting point to help prepare for compliance test. As each system is different there are many features in the DP149 to help tune the circuit. These include V_{OD} adjust by changing the Vsadj resistor value or using I^2C. Other knobs to turn are pre/de-emphasis and slew rate control. Passing HDMI1.4b compliance is easier to accomplish when using I^2C as this provides more fine tuning capability.

For the SNx5DP149RSB:

Pin Strapping

HDMI1.4b

Vsadj Resistor = 6.5 kΩ

PRE_SEL = L for –2 dB

SLEW_CTL = NC

I^2C

HDMI1.4b

Vsadj Resistor = 6.5 kΩ

VSWING_DATA & VSWING_CLK to -7% = Reg0Ch[7:2] = 111111

PRE_SEL = Reg0Ch[1:0] = 00: (Labeled HDMI_TWPST)

TX_TERM_CTL: Reg0Bh[4:3]

- <2 Gbps = 00 for no termination (This may be best value for all HDMI1.4b)
- >2 Gbps and < 3.4 Gbps = 01 for 150 to 300 Ω

SLEW_CTL = Reg0Bh[7:6] = 10

PRODUCT PREVIEW

10 Power Supply Recommendations

10.1 Power Management

To minimize the power consumption of customer application, SNx5DP149 uses dual power supply. V_{CC} is 3.3-V with 10% range to support the I/O voltage. The V_{DD} is 1.00-V to 1.27-V range to supply the internal digital control circuit. SNx5DP149 operates in two different working states. See Table 14 for conditions for each mode. When OE is deasserted and then reasserted the device will rest to its default configurations. If different configurations were programmed using I^2C then the device will have to be reprogrammed.

- Power-down mode:
  - OE = Low puts the device into its lowest power state by shutting down all function blocks
    - When OE is re-asserted the transitions from L → H will create a reset and if the device is programmed through I^2C it will have to be reprogrammed.
    - OE = High, HPD_SNK = Low
    - Writing a 1 to register 09h[3]
- Normal operation: Working in redriver or retimer
- When HPD asserts, the device CDR and output will enable based on the signal detector circuit result
- HPD_SRC = HPD_SNK in all conditions. The HPD channel operational when V_{CC} over 3-V.

Table 14. Control Logic and Mode of Operation

INPUTS(1)		STATUS							MODE
HPD_SNK	OE	Mode of Operation	HPD_SRC	IN_Dx	SDA_CTL SCL_CTL	OUT_Dx OUT_CLK	DDC	AUX_SRC± (48 PIN ONLY)	
H	L	X	H	High-Z	Disabled	High-Z	Disabled	Disable	Power-down mode
L	H	X	L	High-Z	Active	High-Z	Disabled	Disable	Power-down mode
H	H	X	H	High-Z	Active	High-Z	Disabled	Disable	Power-down mode when a one is written to 09h[3]
H	H	Redriver	H	RX active	Active	TX active	Active	Active	Normal operation
H	H	Retimer	H	RX active	Active	TX active	Active	Active	Normal operation

(1) L = LOW, H = HIGH

TMDS output termination control impacts the operating power.

11 Layout

11.1 Layout Guidelines

TI recommends to use at a minimum a four layer stack up to accomplish a low-EMI PCB design. TI recommends six layers because the SNx5DP149 is a two voltage rail device.

- Routing the high-speed input DisplayPort traces and TMDS output traces on the top layer avoids the use of vias (and their discontinuities) and allows for clean interconnects from the HDMI connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit. It is important to match the electrical length of these high speed traces to minimize both inter-pair and intra-pair skew.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.
- The control pin pullup and pulldown resistors are shown in application section for reference. If a high is needed only use the pull up. If a low is needed only use the pull down. If mid level is to be selected do not

Layout Guidelines (continued)

use either resistors and leave the pin floating/No connect.

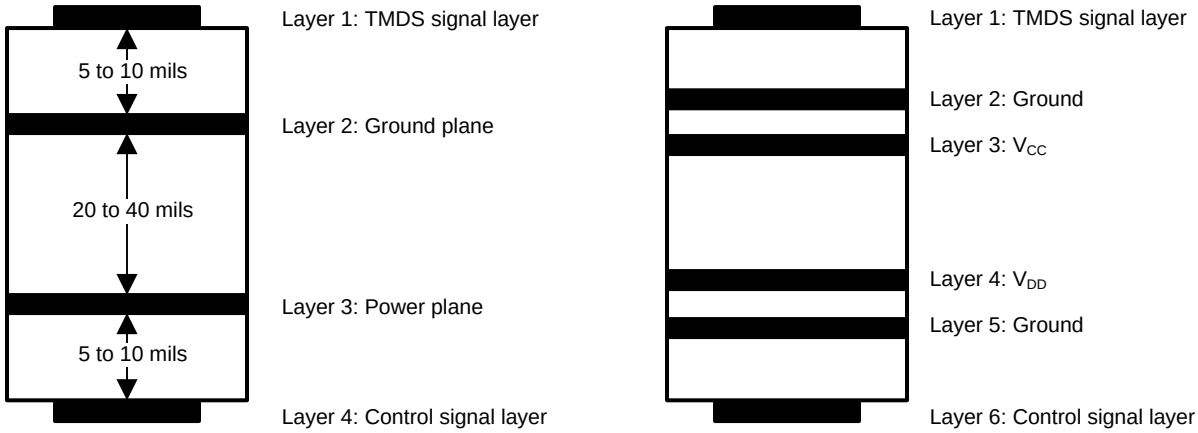

Figure 32. Recommended 4- or 6-Layer Stack for a Receiver PCB Design

11.2 Layout Example

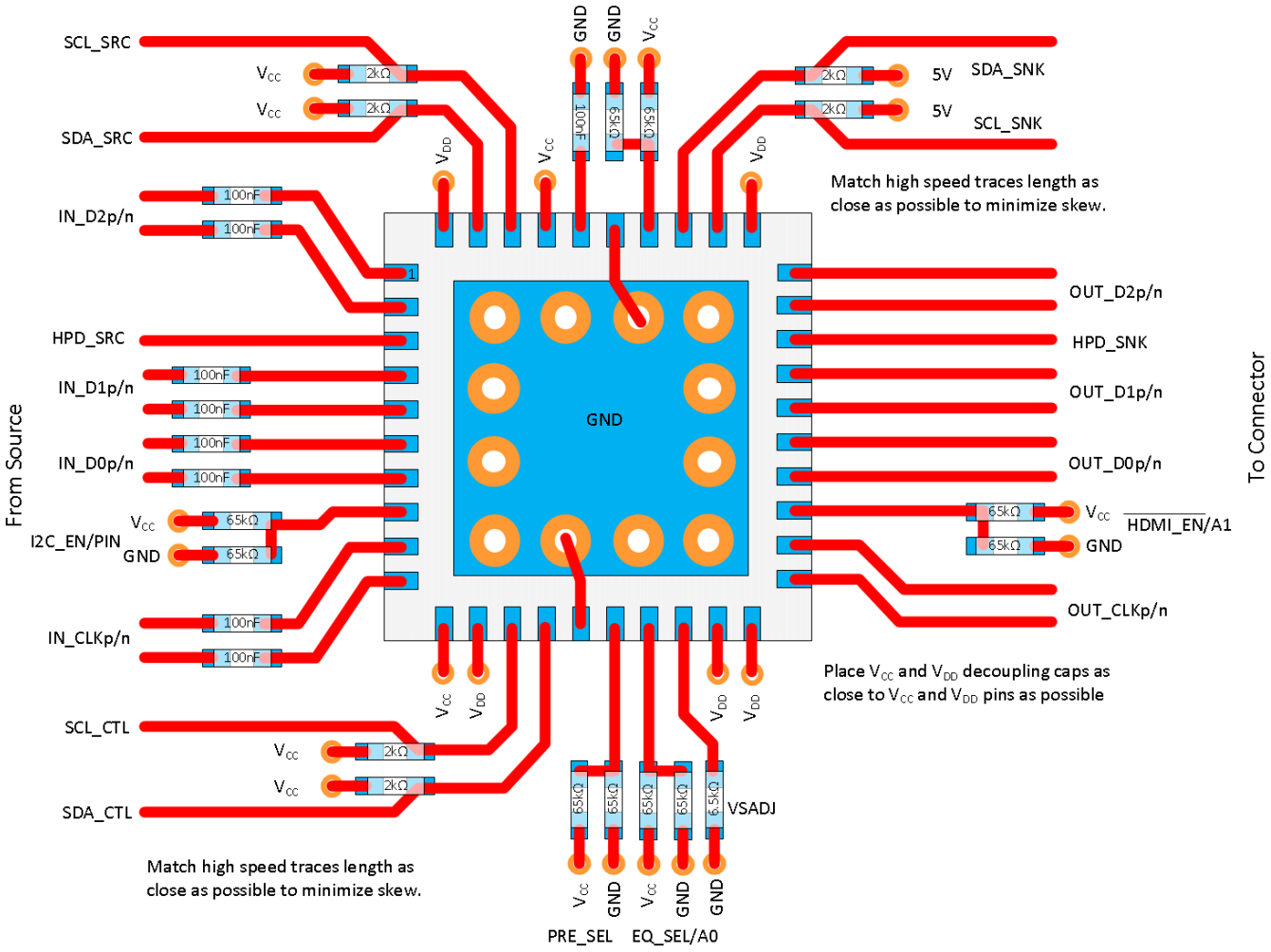

Figure 33. Layout Example for the DP149RSB

11.3 Thermal Considerations

On a high-K board: TI recommends to solder the PowerPAD™ onto the thermal land. A thermal land is the area of solder-tinned-copper underneath the PowerPAD package. On a high-K board, the SNx5DP149 device can operate over the full temperature range by soldering the PowerPAD onto the thermal land without vias.

On a low-K board: For the device to operate across the temperature range on a low-K board, a 1-oz Cu trace connecting the GND pins to the thermal land must be used. A simulation shows $R_{\theta JA}$ = 100.84°C/W allowing 545-mW power dissipation at 70°C ambient temperature.

A general PCB design guide for PowerPAD packages is provided in *PowerPAD Thermally Enhanced Package*, SLMA002.

12 Device and Documentation Support

12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 15. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65DP149	Click here	Click here	Click here	Click here	Click here
SN75DP149	Click here	Click here	Click here	Click here	Click here

12.2 Documentation Support

12.2.1 Related Documentation

The documents identified in this section are referenced within this data sheet. Most references within the data sheet use the text identified within the brackets [Document Tag], instead of the complete document title to simplify the text.

(1) [Dual Mode] VESA DisplayPort Dual-Mode Standard Version 1.1, February 8, 2013
(2) [HDMI1.4b] High-Definition Multimedia Interface Specification Version 1.4b, October, 2011
(3) [HDMI2.0] High-Definition Multimedia Interface Specification Version 2.0a, March, 2015
(4) [I^2C] The I^2C-Bus specification version 2.1, January, 2000
(5) [HDMI1.4b CTS] High-definition Multimedia Interface CTS for Version 1.4b October, 2011
(6) [HDMI2.0 CTS] High-definition Multimedia Interface CTS for Version 2.0k June, 2015

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
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PRODUCT PREVIEW

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65DP149RSBR	PREVIEW	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DP149	
SN65DP149RSBT	PREVIEW	WQFN	RSB	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DP149	
SN75DP149RSBR	PREVIEW	WQFN	RSB	40	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75DP149	
SN75DP149RSBT	PREVIEW	WQFN	RSB	40	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	75DP149	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

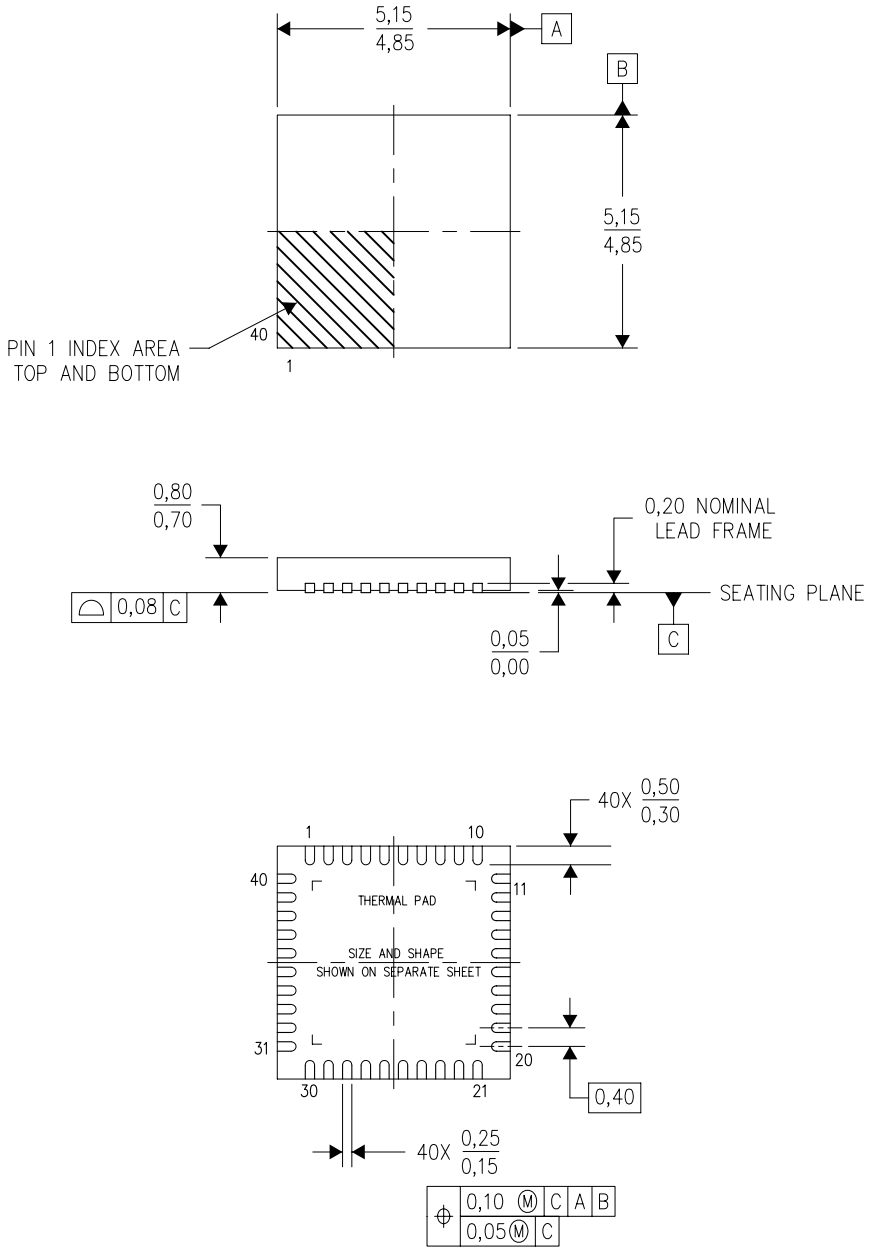
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

RSB (S–PWQFN–N40) PLASTIC QUAD FLATPACK NO–LEAD



4207182/C 05/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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